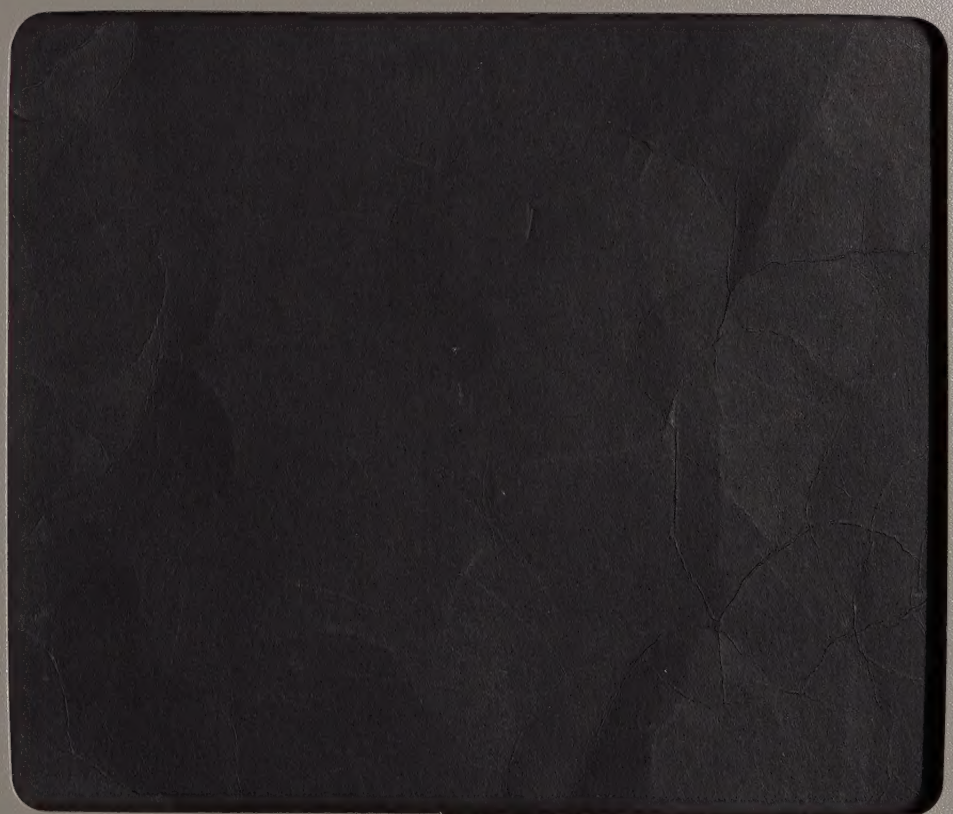
Fluke 7260A

Universal Counter



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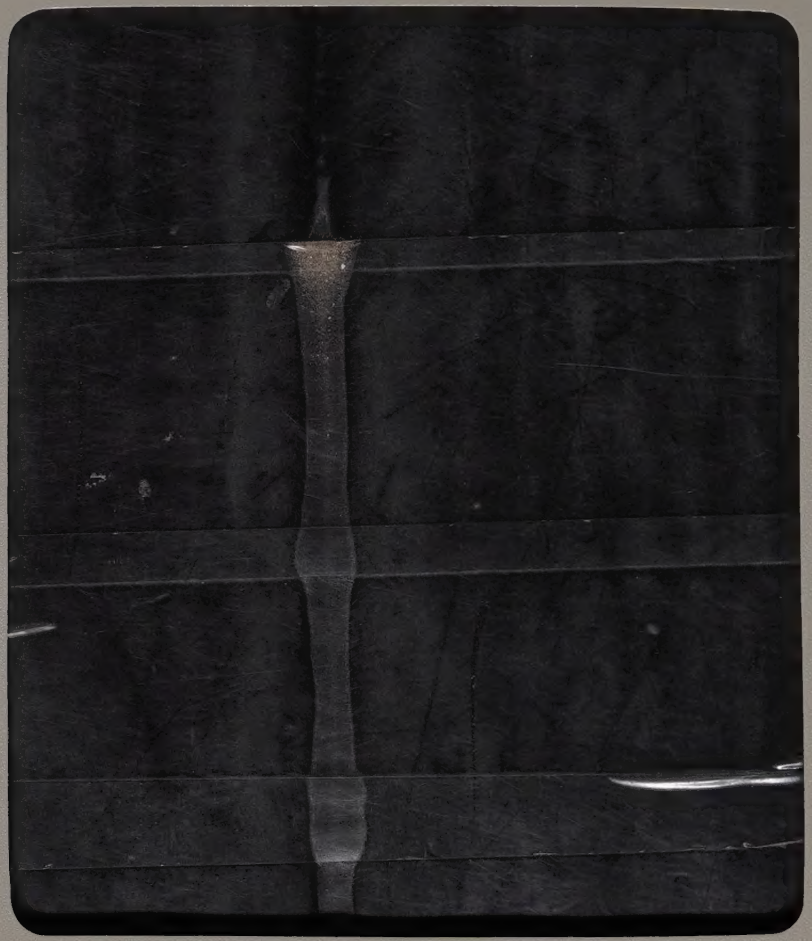

NOTE

This manual documents the Model 7260A and its assemblies at the revision levels shown in Appendix 7A. If your instrument contains assemblies with different revision letters, it will be necessary for you to either update or backdate this manual. Refer to the supplemental change/errata sheet for newer assemblies, or to the backdating sheet in Appendix 7A for older assemblies.

7260A

Universal Counter/Timer

Instruction Manual

P/N 487504
January 1979
Rev. 1 9/80
Rev. 2 2/81

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*For European customers, Air Freight prepaid.

John Fluke Mfg. Co., Inc., P.O. Box C9090, Everett, Washington 98206

Rev. 6/81

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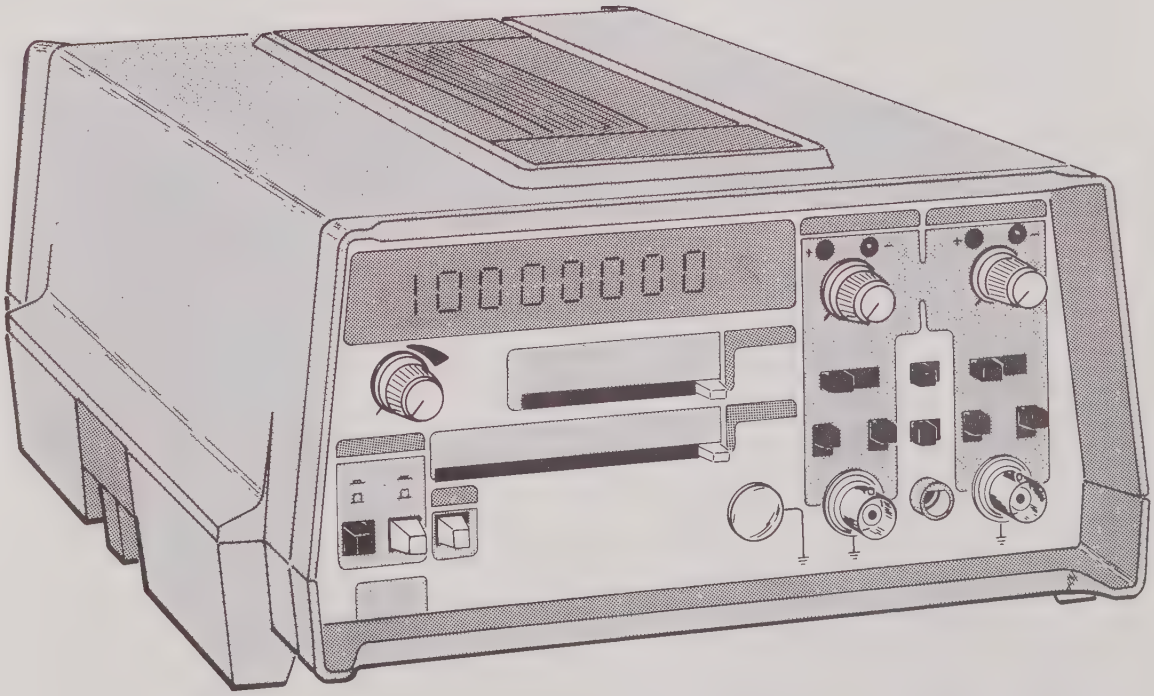


Model 7260A Universal Counter-Timer

Section 1
Introduction & Specifications

1-1. INTRODUCTION

1-2. The Model 7260A is a Universal Counter/Timer capable of displayed measurements in the following 10 modes of operation: frequency (Channel A), Counts per Minute (Channel A), frequency (Channel C with Option-310) ratio (Channel A divided by Channel B), period and period average (Channel A), time interval and time interval average (start on Channel A, stop on Channel B), totalize (Channel A gated by Channel B), and self check.

1-3. This manual will document the 7260A under two categories. The standard instrument without options or accessories will be covered in Section 1-5, 7 and 8. All optional or accessory items will be documented in Section 6. Schematic diagrams for the standard instrument and the options will be centralized in Section 8.

1-4. DESCRIPTION

1-5. The Model 7260A features an eight-digit display with full annunciation, leading zero suppression and autoreset. Decimal point placement and units annunciation are controlled by FUNCTION and RESOLUTION sliding select switches.

1-6. Provision is made for separate or common inputs to CHANNEL A or CHANNEL B. Each of these channels features separate trigger level, attenuation, slope and input coupling controls. A 100 kHz low pass filter may also be activated for both channels.

1-7. Frequency measurements may be made from 0 to 125 MHz. With the Channel C option installed, this range may be extended to 520 MHz. Ratio or totalize inputs to Channel B and Period or Period Average inputs to Channel A can be made to 2 MHz. Time Interval and time interval averaging can be measured to 5 MHz.

1-8. A number of options and accessories are available for use with the 7260A. Increased accuracy can be realized by using one of the optional time bases. A battery pack is available for fully portable operation. Data interchanges with remote interfaces are possible with the Data Input/Output Unit installed. When combined with the Interface PCB Assembly and the 1120A IEEE-488 Translator, the I/O Unit can be used for IEEE-488 bus conversations. Options and Accessories for the 7260A are listed in Tables 1-1 and 1-2 respectively.

1-9. SPECIFICATIONS

1-10. Specifications for the 7260A Universal Counter/Timer are listed in Table 1-3.

Table 1-1. 7260A Options

OPTION NO.	DESCRIPTION
72XXA-010	Internal Battery Pack
72XXA-112	TCXO (2 ppm)
72XXA-131	Low Power Oven
72XXA-132	Superior Low Power Oven Time Base
72XXA-310	520 MHz Direct Channel C
72XXA-331	1300 MHz Prescaler
72XXA-521	Digital Interface PCB
72XXA-522	Interface PCB Assembly
72XXA-529	IEEE Interface

Table 1-2. 7260A Accessories

MODEL NO.	DESCRIPTION
Y2014	C Size Single Unit Offset Rack Mount
Y2015	C Size Dual Rack Mount
Y2020	C Size Panel Mount
Y7201	Filter/Attenuator
Y7203	Instrument Cable, 2 ft. } to 1120A
Y7204	Instrument Cable, 5 ft. } to 1120A

Table 1-3. Specifications

GENERAL	
Display Annunciation	8-digit LED, Leading Zero Suppression sec, msec, μsec, kHz, MHz, Gate, Oven, Overflow.
Autoranging	Automatically selects range that optimizes resolution and measurement time. A 20% hysteresis switching threshold eliminates unnecessary up/down resolution changes.
Reset	Reset switch clears display, lights all display segments; on release, a new measurement is activated.
Self-Check	Uses internal 10 MHz signal to check digital circuits.
Time Base Output	Buffered TTL compatible, 10 MHz signal derived from crystal time base. ⩾.5V into 50Ω.
Marker Output	TTL compatible output. Positive going edge indicates A Channel trigger; negative going edge indicates B Channel trigger. Delay from time signal triggers input amplifier to time marker changes level at the rear panel connector typically = 400 ns. Output level nominally .5V.
Trigger Level Output	±1.5V, indicates DC trigger level set at either Channel A or B, switch selectable.
Time Interval Holdoff	20 μsec -20 msec, continuously adjustable.
Cycle Rate	250 ms fixed between readings.
Operating Temperature (stacked)	0° – 40°C.
Storage Temperature	–40° – +70°C.
Power Requirements	32 VA, maximum.
Line Voltage	100, 120, 220 or 240V ac.
Line Frequency	47 – 63 Hz.
Dimensions	Standard type "C" PTI Case (See Figure 1-1). 10.49 cm H x 32.64 cm L x 20.45 cm W 4.13 in H x 12.85 in L x 8.05 in W
Weight (without Options)	3.1 kg 6 lbs. 14 oz
EMI	Internal metal RFI shield (meets requirements of MIL-STD-461, notice 3).

FUNCTIONS (see footnotes for definiton of terms)	
Frequency A	
Range	0 – 125 MHz
Resolution	.1 Hz – 10 kHz in decade steps.
Accuracy	±1 count ±time base errors.
Display	kHz or MHz with decimal point.
CPM X100A	
Range	0 – 125 MHz.
Resolution	100 CPM, fixed.
Accuracy	±1 count ±time base errors.
Display	No decimal point or annunciators.
Frequency C (Option -310)	
Range	50 MHz – 520 MHz
Resolution	.1 Hz – 10 kHz in decade steps.
Accuracy	±1 count ±time base errors.
Display	kHz or MHz with decimal point.

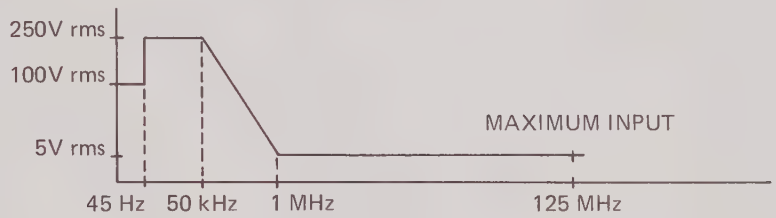
Table 1-3. Specifications (cont)

Ratio A/B	
Range	A: 0 – 125 MHz.
Resolution	B: 0 – 2 MHz.
Resolution	N x A/B
Accuracy	± 1 count $\pm\frac{(\text{Freq A} \times \text{Trig Error B})}{N}$
Display	Decimal point without annunciator.
Period A	
Range	100 ns – 99,999.99 sec (before overflow).
Resolution	100 ns – 10 ms in decade steps.
Accuracy	±1 count ±time base errors ±trigger error.
Frequency	5 Hz – 1 MHz, sine wave
Maximum Rise Time	200 ms, below 5 Hz.
Minimum Pulse	500 ns (5 Hz – 100 kHz) 250 ns (100 kHz – 1 MHz)
Display	msec or sec, with decimal point.
Period Average A	
Range	1 ps – 999,999.9 μs (before overflow)
Resolution	1 ps – 100 ns in decade steps.
Accuracy	$\frac{100\text{ ns}}{N}$ ±time base errors $\pm\frac{\text{trigger error}}{N}$
Frequency Range	5 Hz – 1 MHz, sine wave.
Maximum Rise Time	200 ms, below 5 Hz.
Minimum Pulse	500 ns (5 Hz – 100 kHz) 250 ns (100 kHz – 1 MHz)
Display	μsec or msec, with decimal point.
Time Interval A-B	
Range	100 ns – 99,999.99 sec (before overflow).
Resolution	100 ns – 10 ms in decade steps.
Accuracy	100 ns ±time base errors ±trigger error
Frequency Range	5 Hz – 2 MHz, sine wave.
Maximum Rise Time	200 msec, below 5 Hz.
Minimum Pulse	500 ns, 5 Hz – 100 kHz. 250 ns, 100 kHz – 2 MHz.
Display	msec or sec, with decimal point.
Time Interval Average A-B	
Range	1 ns – 9.9999999 sec, before overflow.
Resolution	$\frac{100\text{ ns},}{\sqrt{N}}$ ($N = 1 - 10^5$ in decade steps)
Accuracy	$\pm\frac{100\text{ ns}}{\sqrt{N}}$ ±10 ns ±time base errors $\pm\frac{\text{trigger error}}{\sqrt{N}}$
Frequency Range	0 – 5 MHz
Minimum Pulse	50 ns
Dead Time	200 nsec (stop to start).
Display	μsec or msec with decimal point.
Totalize A·B	
Range	A: 0-125 MHz B: 0-2 MHz
Count Capacity	0 – 99999999
Display	No decimal point or annunciator.

Table 1-3. Specifications (cont)

SIGNAL INPUTS – CHANNEL A & B

Bandwidth	0 – 125 MHz (DC coupled) 5 – 125 MHz (AC coupled)
Sensitivity	10 mV rms (0 – 50 MHz) 15 mV rms (50 – 100 MHz) 35 mV rms (100 – 125 MHz)
Minimum Pulse	10 ns at 50 mV peak.
Linear Operating Range	+2.5V to –2.5V.
Trigger Level Range	+1.5V to –1.5V.
Input Impedance	1 MΩ shunted by 55 pF nominal.
Coupling	AC or DC, switchable.
Attenuator	X1, X10, X100.
Slope	+ or –, switchable.
Channel Input	Separate or Common, switchable.
Filter	100 kHz (3 dB point).
Time Interval Holdoff	20 μsec – 20 msec, continuously adjustable.



SIGNAL INPUTS – CHANNEL C

Range	50 MHz – 520 MHz (Option -310).
Sensitivity	10 mV rms.
Impedance	50Ω, 2.5:1 VSWR.
Maximum Input Voltage	5V rms, fused.

EXTERNAL TIME BASE INPUT

Frequency Required	10 MHz, AC coupled.
Sensitivity	300 mV rms.
Input Impedance	Nominally 1 kΩ in parallel with 30 pF.
Maximum Input	3V rms.

TIME BASES

STANDARD TIME BASE (10 MHz)

Aging Rate per Month	$\pm 5 \times 10^{-7}$
Stability (0° – 50°C)	$\pm 5 \times 10^{-6}$
Line Voltage (±10%)	$\pm 1 \times 10^{-7}$
Battery	$\pm 1 \times 10^{-7}$

Table 1-3. Specifications (cont)

OPTION TIME BASE (10 MHz)

	TCXO (2 ppm) Option -112	Low Power Oven Option -131	Superior Low Power Oven Option -132
Aging Rate (constant temperature)			
per Day			$\pm 3 \times 10^{-9}$
per Month	$\pm 3 \times 10^{-7}$	$\pm 1 \times 10^{-7}$ *	$\pm 5 \times 10^{-8}$ *
per Year	$\pm 1 \times 10^{-6}$		
Accuracy with Temperature** (0 – 50°C)	$\pm 2 \times 10^{-6}$	$\pm 1 \times 10^{-7}$	$\pm 3 \times 10^{-8}$
Line Voltage (±10%)	$\pm 2 \times 10^{-8}$	$\pm 2 \times 10^{-8}$	$\pm 4 \times 10^{-9}$
Battery	$\pm 2 \times 10^{-8}$	$\pm 5 \times 10^{-8}$	$\pm 1 \times 10^{-8}$
Warmup***			
10 Min		$\pm 5 \times 10^{-7}$	$\pm 5 \times 10^{-7}$
20 Min		$\pm 3 \times 10^{-8}$	$\pm 3 \times 10^{-8}$

* After 5 days continuous operation.

** Accuracy with temperature includes errors caused by temperature variations during operation as well as all calibration errors.

*** This specification defines how close the oscillator will be to the final frequency within the specified time.

BATTERY PACK (OPTION -010)

Operating Time	2.8 hours typical, continuous. Decrease to 2.0 hours typical, worst case with load of options.
Charge Time	16 hours at room temperature.
Battery Type	Nicad, F cells.
Charge Protection	Thermistor actuated shut down of charging circuit if battery temperature exceeds 65°C.
Discharge Protection	Automatic low-voltage shut down to prevent over discharge.

DATA OUTPUT UNIT (OPTION -521)

Description	Serial BCD output of all digits and annunciators.
Levels	TTL, "1" state low.
Speed	60 readings / sec.
Compatibility	For use with Fluke 1120A IEEE Translator.

IEEE INTERFACE (OPTION -529)

Description	Option for interfacing the 7260A to IEEE-488. Option package consists of a board in the 7260A, a ribbon cable and a board for the Fluke 1120A IEEE Translator. The 1120A must be used to interface the 7260A to IEEE-488. Provides full measurement output capability and limited trigger and reset of a measurement.
IEEE Repertoire	SH1, AH1, TE0, L4, LE0, SR1, RL2, PP0, DC1, DT1, C0.

Table 1-3. Specifications (cont)

520 MHz CHANNEL C DIRECT (OPTION -310)	
Description	Provides a third input channel for measuring frequencies from 50 MHz to 520 MHz.
Sensitivity	10 mV rms.
Input Impedance	50Ω, VSWR 2.5:1.
Maximum Input Voltage	5V rms, fuse protected.

FOOTNOTES:

1. *$N = 10^0$ to 10^5 in decade steps set by resolution switch. Indicates the number periods averaged in Period Average or Time Interval Average mode, and the number of cycles of B averaged in Ratio mode.*
2. *Time base error is the sum of all erors specified in the time base section for a particular time base.*
3. *Trigger error is the measurement error caused by noise on the input signal triggering the input amplifier early or late. It is calculated as follows:*

$$\text{Trigger Error} = \left[\pm \frac{2 \times \text{peak noise (V)}}{\text{Signal Slope at Trigger Point (V/}\mu\text{s)}} \mu s \right]$$

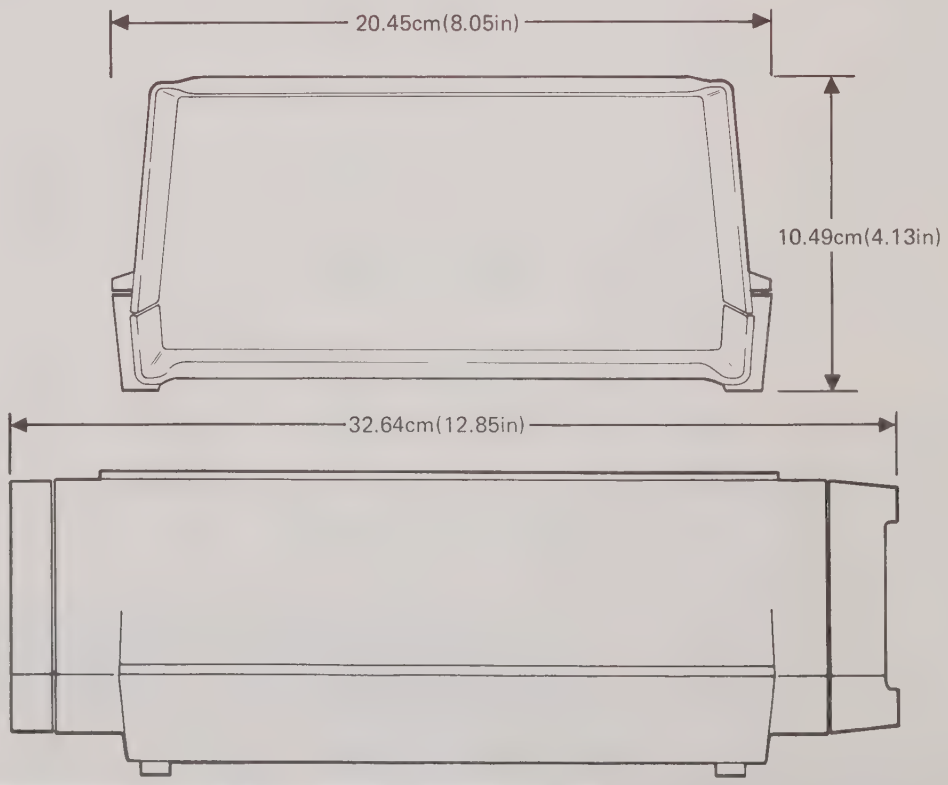
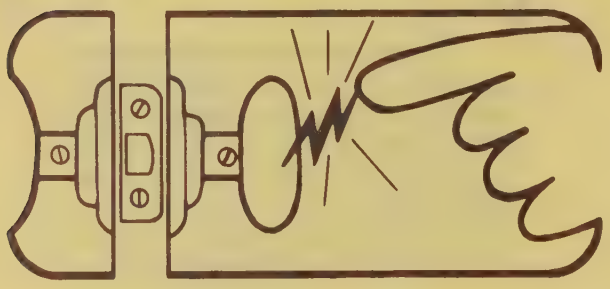


Figure 1-1. Dimensions

static awareness

A Message From

John Fluke Mfg. Co., Inc.

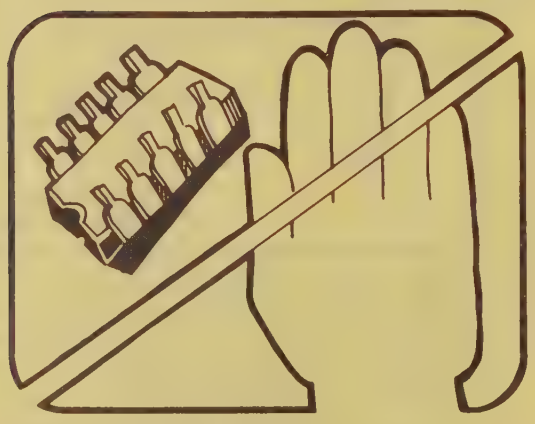


Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

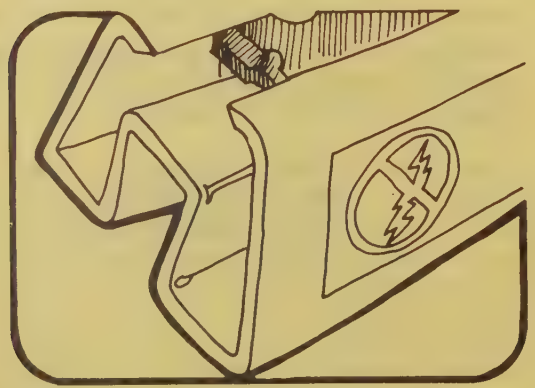
1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol "⊗"

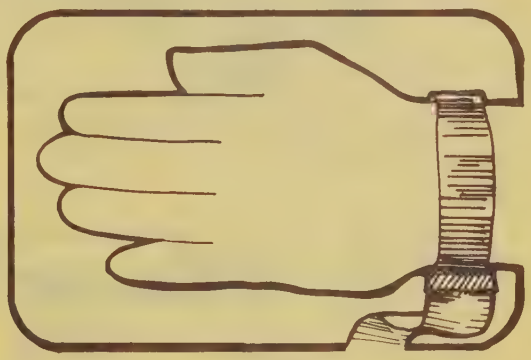
The following practices should be followed to minimize damage to S.S. devices.



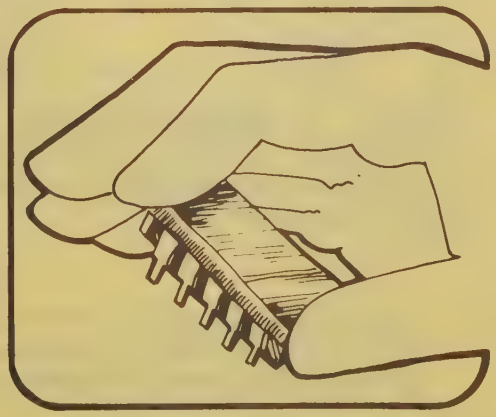
1. MINIMIZE HANDLING



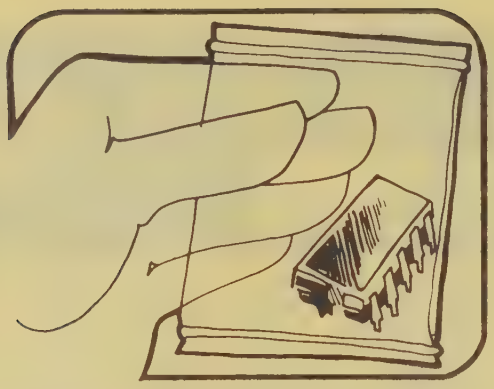
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



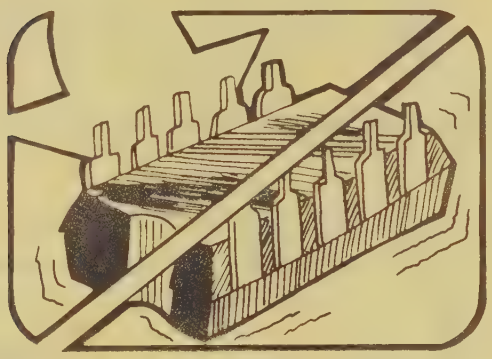
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES. USE A HIGH RESISTANCE GROUNDING WRIST STRAP.



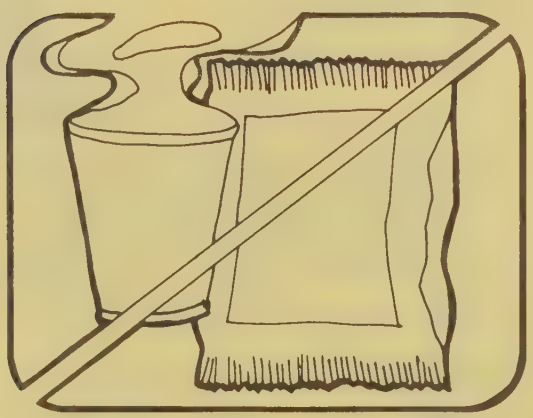
4. HANDLE S.S. DEVICES BY THE BODY



5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT



6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE



7. AVOID PLASTIC, VINYL AND STYROFOAM® IN WORK AREA

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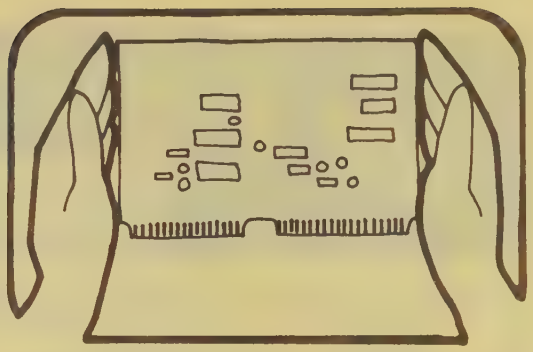
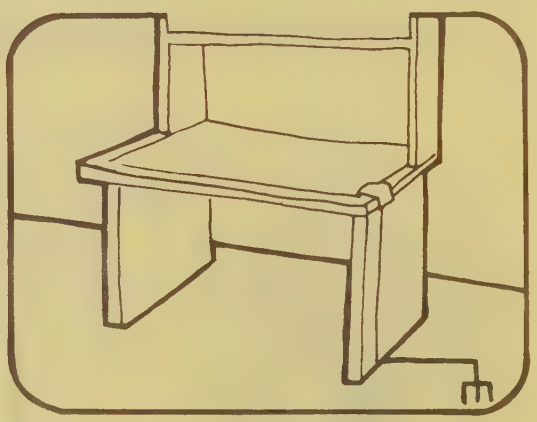
AND GENERAL DYNAMICS, POMONA DIV.



8. WHEN REMOVING PLUG-IN ASSEMBLIES, HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS TO PROTECT INSTALLED SS DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION
10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.
11. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

A complete line of static shielding bags and accessories is available from Fluke Parts Department, Telephone 800-526-4731 or write to:

JOHN FLUKE MFG. CO., INC.
PARTS DEPT. M/S 86
9028 EVERGREEN WAY
EVERETT, WA 98204

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Rev. 1 MAR 86

Section 2
Operating Instructions

2-1. INTRODUCTION

2-2. Installation and operation of the 7260A Universal Counter/Timer are explained in this section. Read this information before attempting to operate the unit. Should any difficulties arise, contact your nearest Fluke Sales Representative (listed in Section 7), or the John Fluke Mfg. Co., Inc. (P.O. Box 43210, Mountlake Terrace, WA., 98043; Telephone 206 774-2211).

2-3. SHIPPING INFORMATION

2-4. The 7260A is packaged and shipped in a foam-packed container. An Instruction Manual and any accessories ordered will be included with the instrument. Upon receipt of the instrument, make a thorough inspection for proper contents and possible shipping damage. Special instructions for inspection and claims are included with the shipping container. If reshipment is necessary, use the original container. If the original container is not available, a new container can be obtained from the John Fluke Mfg. Co., Inc. Please reference the instrument model number when requesting a new shipping container.

2-5. INSTALLATION

2-6. Input Power

2-7. The 7260A can be operated with an input line voltage of 100, 120, 220, or 240V ac (±10%). Line frequency may vary between 47 and 63 Hz. Before connecting the power cord, verify that line voltage switches (located inside the instrument) are properly set and that an appropriate line fuse is installed. Refer to Section 4 of this manual for proper verification procedures (see "Line Voltage Selection" and "Fuse Replacement"). Primary voltage to the power transformer can be controlled with a rear panel switch.

2-8. Instrument Case Mating

2-9. The 7260A is contained in a molded instrument case with non-marring feet, a tilt-down bail, and a latching arrangement. This instrument may be stacked and latched together with other Fluke instruments employing this type of case.

2-10. Use the following procedure when attaching these molded cases together:

1. For the top instrument, pull out latches found on either side (refer to Figure 2-1).
2. Nestle top and bottom instruments together.
3. Push latches in to secure instruments together.

CAUTION

Instrument stacks should be limited to a total height of three feet and a total weight of 40 pounds.

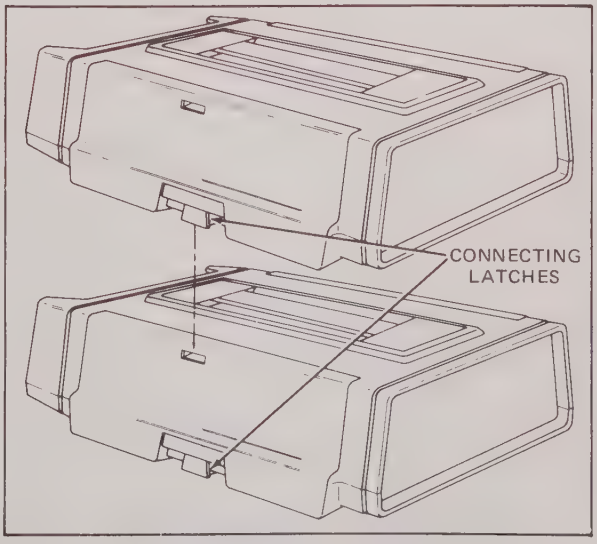


Figure 2-1. Instrument Case Mating

2-11. Tilt-Down Bail

2-12. When used as a separate instrument, the 7260A may be tilted up, or down, with the aid of the tilt bail. When extended, the bail may be locked in place by firmly pressing the legs into slots provided in the bottom panel. When retracted, the bail lies flush with the instrument's bottom panel and does not interfere with case mating. This bail will normally be mounted toward the front of the instrument's bottom panel. To remove the bail, compress either of its legs toward the center of the case and pull out. Installation may then be made in identical mounts at the rear of the bottom panel.

2-13. Rack Installation

2-14. The 7260A may be installed in a standard 19-inch equipment rack or a DIN panel mount. Mounting kits for these accessories are described in Section 6 of this manual. A list of all available accessories and options is presented in Section 1.

2-15. OPERATING FEATURES

2-16. The location of front panel controls, indicators and connectors is shown in Figure 2-2. Referenced by number, these items are briefly described in Table 2-1. Rear panel controls and connectors are covered in a similar fashion in Figure 2-3 and Table 2-2. It is suggested that the operator become acquainted with this information before operating the instrument.

2-17. OPERATING NOTES

2-18. The following paragraphs describe various conditions and information which should be considered before operating the Model 7260A Counter/Timer.

2-19. AC Line Connection

2-20. The input power cord is a three-pin polarized connector which permits connection to any of the power voltages described in INPUT POWER. Ensure that the ground pin is connected to a high quality earth ground.

2-21. Maximum Inputs

WARNING

ALL BNC CONNECTOR SHELLS ON THE 7260A ARE TIED DIRECTLY TO EARTH GROUND THROUGH THE POWER PLUG. DO NOT CONNECT THE ACTIVE LEAD OF THE INPUT SIGNALS TO THE SHELL. IRREPARABLE DAMAGE TO THE INSTRUMENT OR THE SIGNAL SOURCE MAY RESULT.

2-22. Maximum allowable signal level inputs for each input terminal are specified in Section 1. Channels A and B are fused at 250 mA for fire prevention. Refer to Section 4 of this manual for fuse replacement instructions.

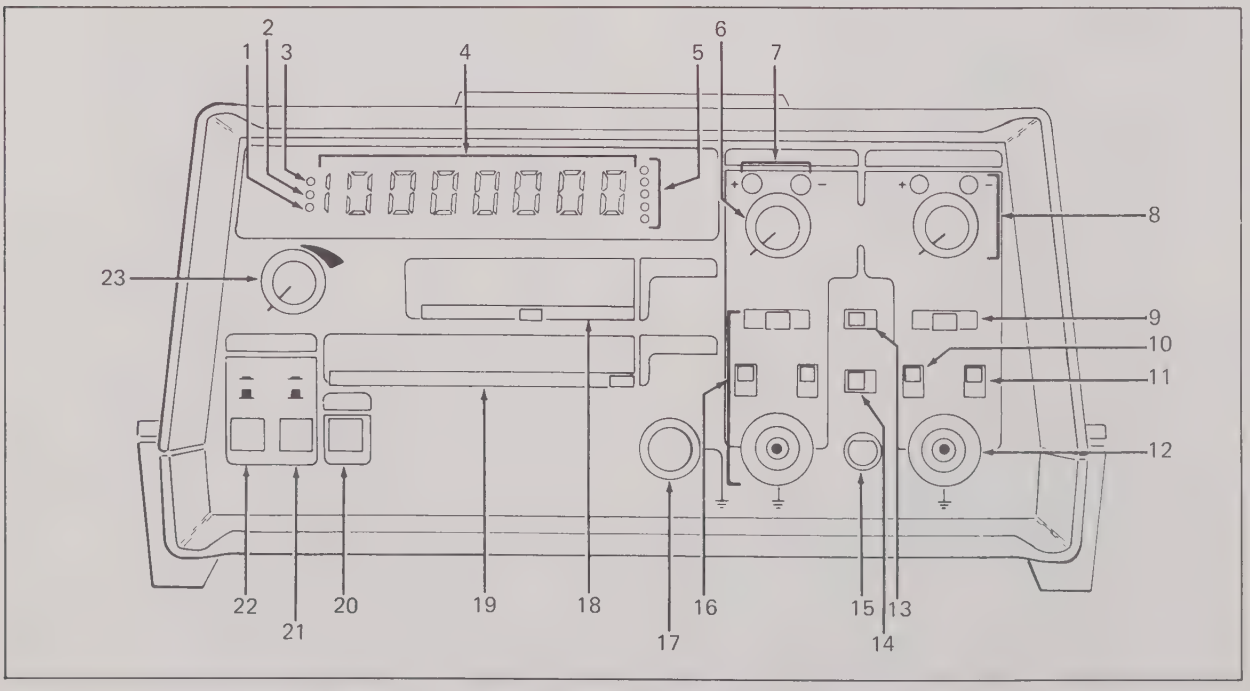


Figure 2-2. Front Panel Controls, Connectors and Indicators

Table 2-1. 7260A Front Panel Controls, Connectors and Indicators

REF NO.	NAME	DESCRIPTION
1	Oven Indicator	If an oven time base (Option -131 or -132) is installed, OVEN is illuminated when the time base is receiving power.
2	Overflow Indicator	Illuminates when the capacity of the display has been exceeded.
3	Gate Indicator	Illuminates when the Main Gate has been enabled. Flashes at a discernible rate when gating is in progress.
4	Display	Eight digit LED readout of measured value. May range from 00000000 to 99999999 with decimal point placement. Leading zero suppression.
5	Units Annunciator	One of five LED's illuminates in all functions except CPM, RATIO and TOT.
6	Trigger Level Control, Channel A	Selects zero volts (PRESET) or continuously adjustable trigger level from −1.5V to +1.5V.
7	Trigger Indicators, Channel A	Indicates input signal relationship to trigger level. (−) on when signal is below level. (+) on when signal is above level. Both on when instrument is triggering on and off properly.
8	Trigger Level Control and Indicators, Channel B	Performs same functions as 6 and 7.
9	Attenuation Control, Channel B	Three position slide switch used to limit input signal to within instrument's linear range. X10 position divides input signal by 10; X100 by 100.
10	Input Coupling Control, Channel B	Selects AC or DC input signal coupling.
11	Slope Control, Channel B	Two position slide switch selects negative or positive going signal slope for triggering on Channel B.
12	Input Connector, Channel B	BNC connector used to apply input signal to Channel B. 1 MΩ input impedance with maximum input of 250V rms.
13	Separate/Common Signal	Two position slide switch determines input signal routing. In SEP, Channels A and B input signals are isolated from each other and separately controlled. In COM, only Channel A input connector remains active; A input is now applied to circuitry of both channels.
14	Filter Control	A two position slide switch places a 100 kHz low pass filter in series with inputs to both channels (IN).
15	Accessory	Three pin connector supplies voltage and ground to accessory items.
16	Channel A Input Connector and Controls	Performs same functions as 9, 10, 11 and 12.
17	Channel C Input Connector	BNC connector input to Channel C option (fuse protected). Input impedance of 50 ohms; maximum input 5V rms.
18	Function Control	Ten position slide switch determines instrument's measurement function. Any position change will reset the instrument.
19	Resolution Control	Seven position slide switch determines display resolution. In conjunction with function settings, will determine decimal point placement and units annunciator illumination. Any change in switch position automatically resets the instrument.
20	Reset Control	Momentary contact control provides manual reset. Display will read all "8's" while this switch is held depressed in any selected function.
21	Power Source Control	Push-on, push-off selects power from ac line or installed Battery Option (-010). This switch is internally bypassed when the Battery option is not installed.
22	Power Switch	Push-on, push-off applies power to instrument circuitry. In STBY, power to any installed oven time base (-131 or -132) is maintained.
23	Time Interval Holdoff Control	During time interval measurements, this control allows for an adjustable time delay in the generation of the stop pulse from Channel B.

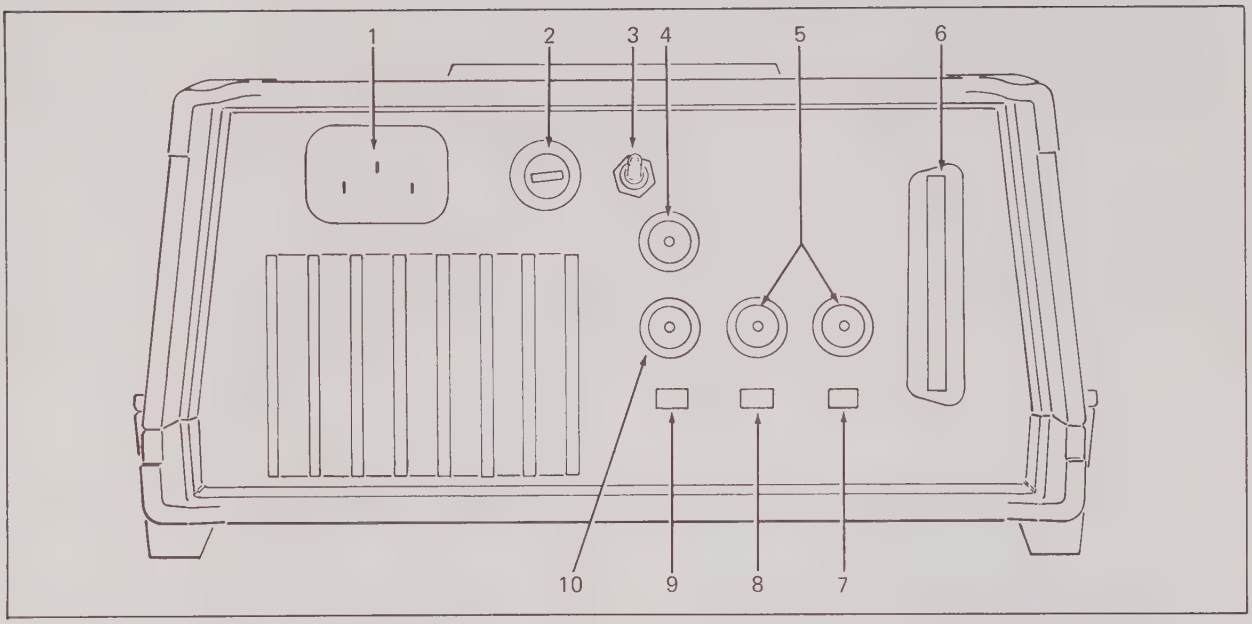


Figure 2-3. Rear Panel Controls and Connectors

Table 2-2. 7260A Rear Panel Controls and Connectors

REF NO.	NAME	DESCRIPTION
1	Power Receptacle	Polarized, 3-pin connector for ac line input.
2	F1	Main Power Fuse.
3	AC Power Switch	Connects (ON) or disconnects (OFF) line power to the primary side of the Main Power Transformer.
4	Marker Out Connector	Provides marker pulse output during TI or TIA functions to assist operator in setting trigger levels.
5	10 MHz REF IN	BNC terminal allows connection of a 10 MHz external time base (switch in EXT).
	OUT	BNC terminal supplies 10 MHz time base signal used by the instrument.
6	DATA I/O	Connector accessible here for Data Input/Output Unit, Option -521.
7	Reference Select Switch	Two position slide switch to select time base source for the instrument. INT position selects installed time base. EXT position selects external time base connected to the 10 MHz IN terminal.
		NOTE *The EXT position for the reference switch removes power to any installed oven time base (Option -131 or -132).*
8	Mode Select Switch	Two position slide switch determines triggering mode for the instrument. CONT position selects continuous triggering. TRIG position selects single triggering.
9	Trigger Level Select Switch	Two position slide switch selects the channel to be monitored at TRIGGER LEVEL OUT BNC.
10	Trigger Level Out Connector	BNC connector supplies the trigger level of the channel selected by the Trigger Level Select Switch.

2-23. Counter/Timer Terminology

2-24. The following definitions are useful in understanding how and when to use the 7260A controls.

2-25. ATTENUATION

2-26. Attenuation is used to limit the input signal within the input amplifier's linear range. On the 7260A, an attenuation control is provided to limit the input amplifier's gain. The ATTEN control provides three selectable attenuation factors: X1, X10 and X100.

2-27. CYCLE RATE

2-28. This term refers to the minimum time necessary for the instrument to process and display a measurement. It does not include the actual measurement time. In the 7260A, each cycle time is 250 ms.

2-29. DISTORTION

2-30. Distortion results from harmonic or spurious contents on the input waveform.

2-31. DUTY CYCLE

2-32. Duty cycle specifies the ratio of signal on time to off time. The greater the percentage of off time, the lower the duty cycle. Measure low duty cycle signals with dc-coupling selected (AC/DC switch in the DC position).

2-33. EVENT COUNTING

2-34. The accumulation of a number of events over a period of time is termed event counting. Several 7260A functions perform this operation. The FREQ A mode counts events for a specific length of time to determine the Channel A input frequency. In the CPM mode, the Channel A input frequency is counted in the same manner; the duration of the count is changed to normalize the frequency (counts per second) into counts per minute. In TOT A·B mode, a continuously updated count of events on Channel A gated by events on Channel B is displayed. Finally, in RATIO A/B mode, the 7260A will count events on Channel A during a gate time determined by the signal on Channel B. The instrument can measure events generated by a wide variety of sources. For example, the FREQ A function can be used to measure the precision frequency output of a signal synthesizer, and the CPM function can be used to determine the rotational speed of a conveyor belt spindle.

2-35. When using any function that counts events, the instrument must trigger once, and only once, for each event. Use of the front panel controls must be directed toward this end. Noise must be filtered or attenuated to prevent false triggering, and the input signal must be kept within the linear range of the instrument.

2-36. EVENT TIMING

2-37. During event timing functions, an internal oscillator frequency is counted for a period determined by the input signal. In the 7260A, two types of event timing measurements can be made: period and time interval. Period measurement (PER A or PER AVG A) determines the period, or inverse of frequency, of a repetitive signal. The instrument measures period by counting the internal time base frequency for single (PER A) or multiple (PER AVG A) cycles of the input. Time interval measurements (TI A-B) can be made to determine the period of time between any two events, repetitive or not. Average time interval measurements (TIA A-B) can be made on signals with repetitive time intervals. For either type of event timing, separate start and stop signals must be generated from the input (refer to Figure 2-4).

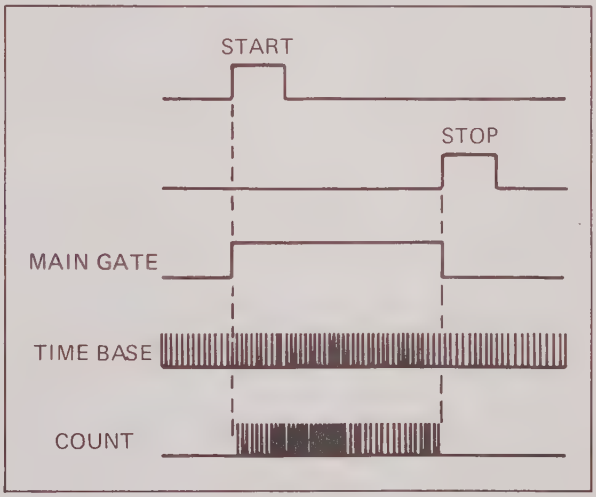


Figure 2-4. Event Timing

2-38. TIME INTERVAL REPETITION RATES (ASYNCHRONOUS VERSUS SYNCHRONOUS)

2-39. Time Interval Averaging is a statistical reduction of both the time base and trigger errors. Like all true statistical functions, Time Interval Averaging depends upon random sampling. If the repetition rate of the time interval is synchronous with the clock used, time interval averaging may not yield the increase in accuracy and resolution expected. The repetition rate is synchronous with the clock if the time interval always starts in the same place with respect to the clock. As Figure 2-5 shows, asynchronous repetition rates can start anywhere, but synchronous repetition rates have a fixed relationship to the clock.

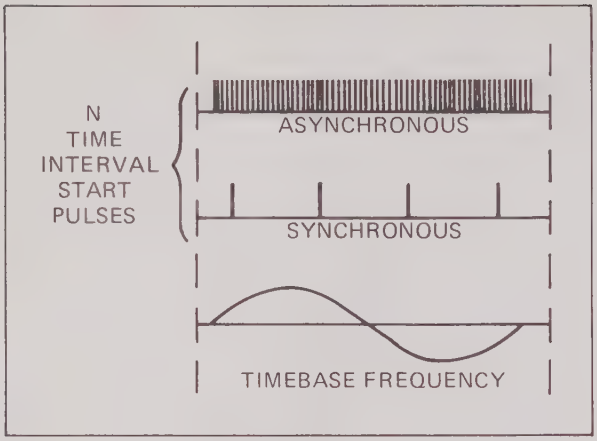


Figure 2-5. Time Interval Repetition Rate Versus Time Base

2-40. GATE TIME

2-41. Gate time refers to the length of time during which a frequency is being counted for display. The frequency counted may be derived from the input signal or from the instrument's internal time base. With longer gate times, more counts are accumulated and measurement resolution improves.

2-42. HYSTERESIS

2-43. In instruments such as the 7260A, proper counting and timing requires a pulsed output from the input circuitry. To form this pulse, each input waveform (regardless of its shape) triggers the input circuitry on or off at predetermined triggering, or hysteresis, levels. An input waveform must pass through both of these hysteresis levels for the input circuitry to generate a pulse. The voltage difference between the two levels is termed the hysteresis window; the minimum signal that can trigger both levels therefore defines the instrument's sensitivity. Generation of the hysteresis window is illustrated in Figure 2-6.

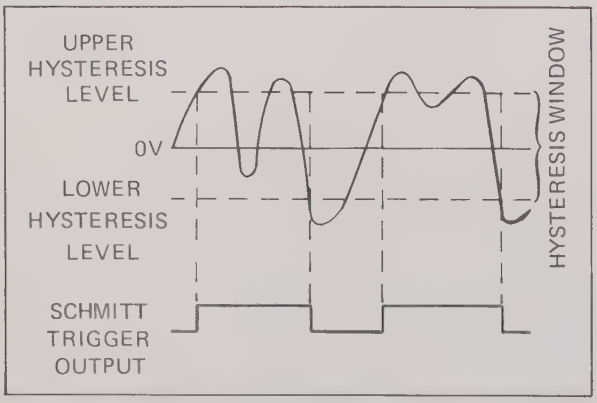


Figure 2-6. Hysteresis Window

2-44. INPUT COUPLING

2-45. Either ac or dc coupling may be used to transfer the input signal to the input conditioning circuitry. An input signal riding on a dc level may not lie within the range of the hysteresis window. The top waveform in Figure 2-7 shows such a dc-coupled waveform. The lower waveform shows the same waveform ac-coupled. With ac-coupling the signal can be measured. AC-coupling causes no problems for repetitive signals of a fixed frequency. The trigger points, however, will shift with a change in frequency or duty cycle. While not important in event counting, such changes are very important to event timing. Pulse inputs with low duty cycles should not be ac-coupled as the coupling capacitor will not charge high enough for proper triggering.

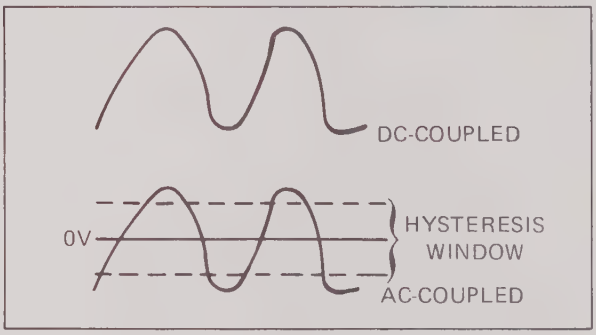


Figure 2-7. Input Coupling

2-46. INPUT IMPEDANCE

2-47. The input impedance defines the impedance seen by a signal source. Input impedance of Channels A and B is 1 MΩ shunted by 55 pF. The optional Channel C input impedance is 50Ω.

2-48. LINEAR OPERATING RANGE

2-49. The linear operating range refers to the excursions of the input signal that can reliably trigger the input amplifier without distortion. The 7260A's linear range varies between the smallest signal level acceptable by the input amplifier (minimum) and the largest attenuated signal that will not be clamped by the amplifier's input circuits (maximum). The minimum is defined by the instrument's sensitivity specifications. Operation within maximum levels may be ensured through proper use of the ATTENUATION controls.

2-50. NOISE

2-51. Noise is defined as spurious signals riding on the input waveform. Unlike distortion, the waveform is not changed. Noise of sufficient amplitude can, however,

cause false triggering, resulting in inaccurate measurements during event timing functions. The 7260A input amplifiers (signal conditioners) exhibit very low noise. The signal applied to these amplifiers may, however, be plagued with noise from the signal source or the electrical environment. Figure 2-8 illustrates effects of noise and distortion.

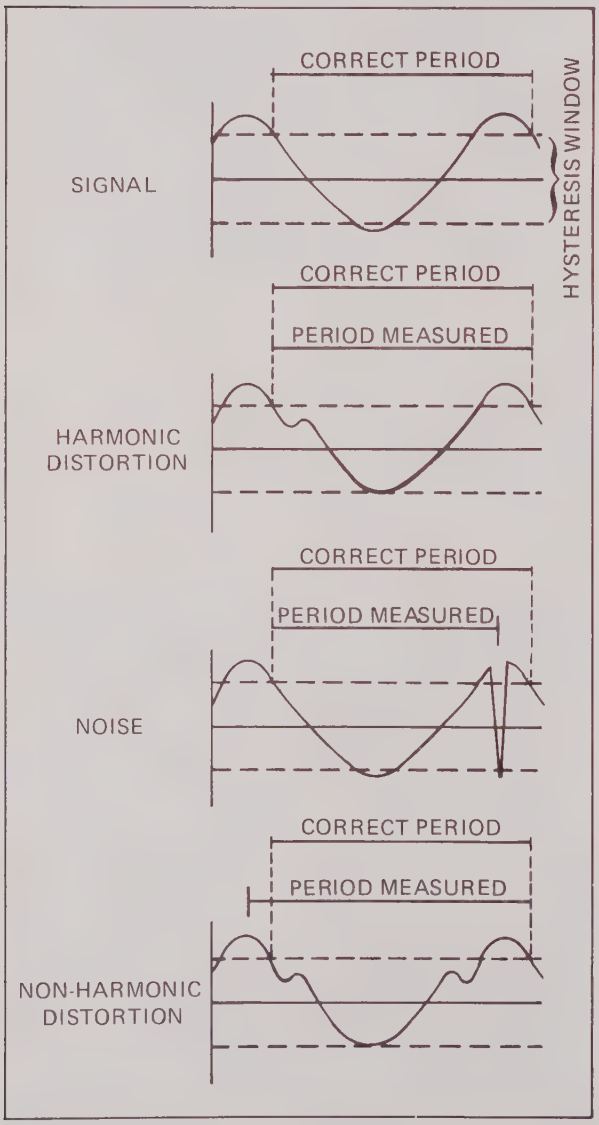


Figure 2-8. Noise and Distortion Effects

2-52. ONE COUNT ERROR

2-53. The one count ambiguity, inherent in any gate and counter type of frequency meter, results from an out-of-phase relationship between the input signal and the internal oscillator signal. The effect is demonstrated in Figure 2-9. During a one second gate time, the top 9.5 Hz signal accumulates a count of ten; during the same gate time, the phase-shifted bottom signal accumulates only nine counts. The ambiguity amounts to one displayed count.

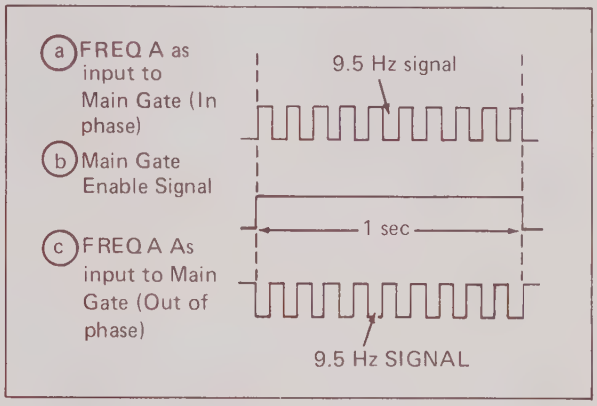

a FREQ A as input to Main Gate (In phase)
b Main Gate Enable Signal
c FREQ A As input to Main Gate (Out of phase)
9.5 Hz signal
1 sec
9.5 Hz SIGNAL

Figure 2-9. One Count Error

2-54. RESOLUTION

2-55. This term defines the value of the smallest displayed unit in a measurement. In the 7260A, this unit (the least significant digit, or LSD) is defined by each combined setting of the FUNCTION and RESOLUTION controls.

2-56. SENSITIVITY

2-57. Sensitivity defines the smallest signal amplitude capable of triggering the instrument. This specification corresponds to an rms value of the peak-to-peak difference between hysteresis levels (the hysteresis window). Note that the waveform must pass both hysteresis levels before a count is generated from the input circuitry; false triggering from noise or distortion on the input signal is thereby minimized.

2-58. TIME BASE ERROR

2-59. Time base error stems from crystal aging, temperature variation, and line voltage fluctuation. The 7260A may be fitted with one of several available time base oscillators; specifications for each are included in Section 1 of this manual.

2-60. TRIGGER ERROR

2-61. Input signal irregularities (noise, distortion, etc.) may cause premature or delayed triggering at the input circuitry's hysteresis levels. During event counting functions, this error is significant only when extra pulses

are generated by the input circuitry. In event timing functions, triggering error may be significant; improper triggering translates into inaccurate counting of the internal oscillator frequency.

2-62. TRIGGERING

2-63. Signal conditioning circuits ideally provide a pulse train output representative of the input signal. These pulses should occur at the same frequency in Event Counting functions. The pulses provide the Start or Stop times in Event Timing functions and must have the same time relationship as the input signals. Each pulse is triggered on and off at the specified upper and lower hysteresis levels for the instrument.

2-64. TRIGGER LEVEL

2-65. The voltage level nominally halfway between upper and lower hysteresis levels is termed the trigger level. On the 7260A, the ATTEN control reduces the input signal within the linear range of the input amplifier. The TRIGGER LEVEL and slope (±) controls then select the trigger level as illustrated in Figure 2-10. Channel A and B trigger levels can be monitored at the rear panel TRIGGER LEVEL OUT connector.

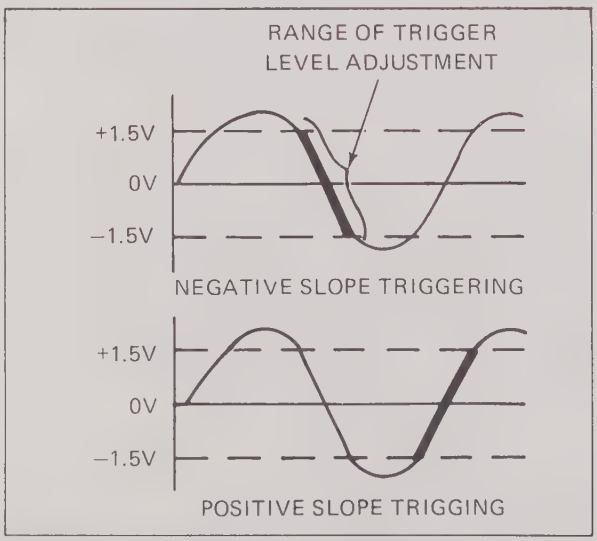


Figure 2-10. Trigger Level

2-66. Function Control

2-67. The FUNCTION slide switch determines the type of measurement that the instrument will make. Each change of the switch position generates an internal reset. The 7260A can measure frequency on Channel A from 0 through 125 MHz when set to FREQ A. The CPM X100A setting displays the Channel A Input (0-125 MHz) as counts per minute times 100. Signal frequency on channel C can be measured when an optional assembly is installed and FREQ C is selected. With RATIO A/B selected, the frequency of Channel A (0-125 MHz) is divided by that of Channel B (0-2 MHz) to yield a numeric ratio. The elapsed time during one or more periods of the input on Channel A can be measured in PER or PER AVG settings (0-2 MHz). The interval in time between an event arriving on Channel A and one on Channel B can be measured over a range of 0-5 MHz with TI A-B selected. The average value of a number of such intervals can be determined and displayed when set to TIA A-B. With TOT A·B selected, a number of events occurring on Channel A can be counted and displayed during a duration of time determined by the input on Channel B. The CHK setting provides a displayed measurement of the intrument's 10 MHz time base to verify digital and display circuit operation.

2-68. Resolution Control

2-69. The front panel RESOLUTION control selects autoranging or one of six manual ranges. Each of these settings is defined by three function-related scales. The scale used is discussed with the appropriate OPERATING DIRECTIONS in this section.

2-70. The RESOLUTION control will have no effect in two functions. For totalizing measurements (TOT A·B), resolution is set at the least significant integer. On the counts per minute mode (CPM X100A), resolution is determined by dividing the number of counts per revolution by the number of minutes. If a 100 count-per-revolution input is used, resolution will translate directly to one RPM.

2-71. When placed in AUTO, the 7260A will automatically step through a predetermined series of resolution settings. The settings available for each function are defined in Table 2-3. When autoranging, the instrument seeks the greatest resolution possible, without overflow, for the function selected and the signal being measured. As an example, with FREQ A selected, the 7260A will step through the first four resolutions to maximize its display capacity when measuring a frequency of 1.2 MHz: the reading will be "1200.000 kHz". If a 1200 Hz signal is measured, maximum resolution allowable will again be found at the last step, but the reading will be "1.200 kHz".

NOTE

During autoranging in the PER A mode, the GATE LED may flash more than once for each display update.

Table 2-4. Autoranging

	10^0 10 kHz	10^1 1 kHz	10^2 100 Hz	10^3 10 Hz	10^4 1 Hz	10^5 0.1 Hz
FREQ A	———	———	———	———	———	
RATIO A/B		———	———	———	———	———
PER A	———	———	———	———		
PER AVG A	———	———	———	———	———	
TI A-B	———	———	———	———		
TIA A-B	———	———	———	———	———	
CHK	———	———	———	———	———	

Autoranging not used in TOT A-B or CPM X100A modes.

Autoranging in RATIO A/B mode will attempt to fill the 7th digit.

2-72. Separate/Common Control

2-73. The SEP/COM control is used to select the input for Channel B's input circuitry. In SEP, the Channel B input connector is tied to the Channel B amplifier and all Channel B controls influence the Channel B signal. In COM, the Channel A signal is used as the input signal to both Channel A and Channel B amplifiers. The Channel A ATTENUATION and AC/DC controls now influence the signal to both amplifiers. All other Channel B controls affect the Channel B applied signal in the normal manner. The switch will be left in the SEP position for most types of measurements. For time interval measurements made on one signal, the COM position should be used. Differing trigger levels could then be set for Channel A and Channel B to determine such factors as rise time and fall time.

NOTE

In COM, the Channel B input is not connected.

2-74. Attenuation Control

2-75. The ATTEN control is a three position switch that can limit instrument input circuit gain by factors of X1, X10 and X100. Large signals causing distortion or non-linear operation can therefore be reduced to within the instrument's linear range. Increased attenuation may also be used to compensate for noise on the input signal; use of ATTEN in this case can prevent the noise from crossing both hysteresis levels.

2-76. Slope Control

2-77. The slope (±) controls determine instrument triggering order for each channel. The initial trigger may occur on a negative going signal (–position) or on a positive going signal (+position). When used together in time interval measurements, the slope controls can define specific portions of a measurement (e.g., pulse width or off time).

2-78. Filter Control

2-79. The position of the Filter IN/OUT switch determines whether or not frequencies above 100 kHz are removed from the input signal for both Channels A and B. When the control is at the IN position, the upper bandpass limit of the input amplifier on the Preamplifier is lowered from 125 MHz to 100 kHz. If high frequency noise is a problem with a low frequency signal, the 100 kHz low pass filter may be used to advantage.

2-80. Trigger Level Control

2-81. The trigger level for either Channel A or Channel B can be selected with the appropriate TRIGGER

LEVEL control. When set fully counterclockwise, the control is in the PRESET state and the trigger level is set at 0V. Clockwise adjustment of the PRESET position will then vary the trigger level continuously from –1.5V to +1.5V. As illustrated in Figure 2-10, the position of this control in conjunction with the slope control determines instrument triggering on the positive or negative slope of the waveform. Exact trigger levels can be monitored at the Rear Panel Trigger Level Out Terminal. The PRESET position generally provides the most sensitive level for ac-coupled symmetrical inputs.

2-82. A coarse indication of triggering level is provided by the two LEDs associated with each Channel. Generally speaking, the + indicator will flash for triggering at a positive trigger level. The same is true for the – indicator and negative triggering levels. Near a zero volt trigger level, both indicators will blink with about the same intensity. Rotation away from this position will cause the opposite polarity LED to slowly fade.

2-83. TI Holdoff Control

2-84. The TI Holdoff control provides a continuously adjustable time delay in generating the STOP pulse during time interval measurements. The operator can thereby selectively measure the time interval between specific pulses in a complex pulse train. Compensation for noise, such as that created by relay contact bounce, may also be made. As an example, Figure 2-11 shows the waveform of a signal generated by relay contact closure. Without TI HOLDOFF actuated, noise from contact bounce is so great that Channel B generates premature stop pulses. With TI HOLDOFF turned on, the start pulse is elongated for a period greater than that of the contact bounce noise. The next Channel B pulse will now generate an accurate STOP pulse. The holdoff period is continuously adjustable from 20 μs to more than 20 ms.

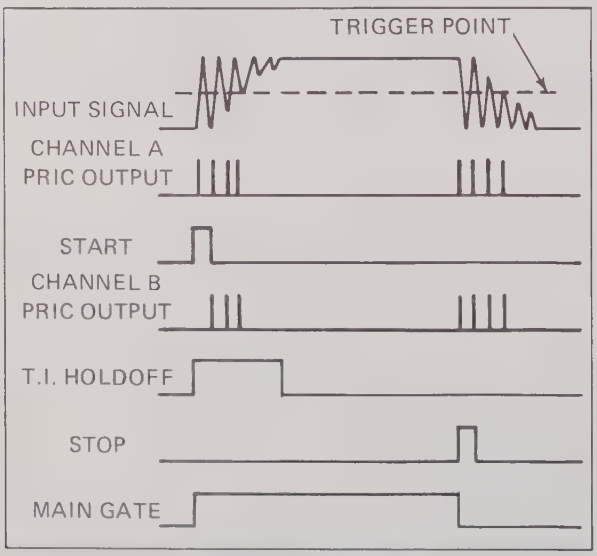


Figure 2-11. TI Holdoff

2-85. Display

2-86. The 7260A display presents an eight-digit LED readout with leading zero suppression. Measurement unit annunciators of MHz or kHz will be activated in FREQ A or CHK modes. For PER A, PER AVG A, TI A-B or TIA A-B, annunciators for μsec, msec, or sec will illuminate. There will be no units annunciation in RATIO A/B, TOT A·B, or CPM X100A modes. Decimal point placement is determined by RESOLUTION and FUNCTION settings, as defined by Figure 2-12.

2-87. There are three status annunciators. The GATE annunciator provides an indication of counting or timing in progress. The OVFL annunciator will illuminate when the capacity of the internal 8-decade accumulator is exceeded. The OVEN annunciator should be on whenever an oven oscillator (Option -131 or -132) is installed, the instrument is connected to line or battery power (STBY or ON), and the Rear Panel REF switch is in the INT position.

2-88. Trigger Mode Control

2-89. With the rear panel trigger MODE control positioned to CONT, the instrument's internal logic will automatically cycle through repetitive measurement routines. When placed in TRIG, a measurement on Channel A can be initiated by using the Channel B signal as a trigger. If the 7260A is in TRIG during remote control operations with the DATA I/O Option -521 installed, refer to Section 6 for special instructions.

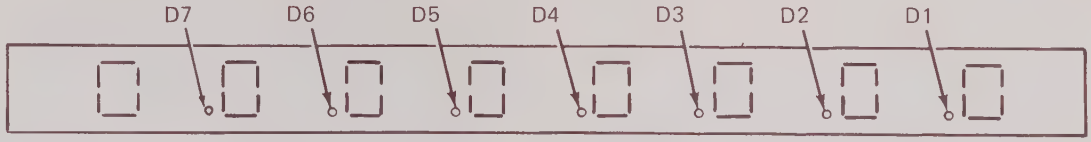
2-90. Remote Operation

2-91. The 7260A can talk and listen to remote stations when fitted with the Data I/O unit (Option -521). The remote stations programming can duplicate the use of the FUNCTION, RESOLUTION, FILTER, slope and RESET front panel controls. The 7260A will respond with measurement data, strobes, decimal points, gate, overflow and units annunciators, and command functions. The Data I/O Unit and interfacing options are documented in Section 6.

2-92. Accuracy

2-93. Techniques are available for improving the accuracy of any measurement. Even with the controls set for optimum performance, three error factors may degrade accuracy. These errors (one count error, trigger error, and time base error) relate to each function as defined in the following accuracy statement:

1. FREQ A, FREQ C, CPM X100A: ±1 count ± Time Base Error



	RESOLUTION						
	10^0	10^1	10^2	10^3	10^4	10^5	
	100 ns	1 μs	10 μs	100 μs	1 ms	10 ms	AUTO
	10 kHz	1 kHz	100Hz	10 Hz	1 Hz	0.1 Hz	
FREQ A	D2	D3	D4	D2	D3	D4	D3
FREQ C	D2	D3	D4	D2	D3	D4	D3
RATIO A/B	–	D1	D2	D3	D4	D5	–
PER A	D4	D3	D2	D4	D3	D2	D3
PER AVG A	D4	D5	D3	D4	D5	D6	D6
T.I. A–B	D4	D3	D2	D4	D3	D2	D3
T.I.A. A–B	D4	D5	D3	D4	D5	D6	D6
CHK	D2	D3	D4	D2	D3	D4	

Figure 2-12. Decimal Point Placement

2. RATIO A/B

$$\pm 1 \text{ count A} \pm \frac{\text{Frequency A (Trigger Error B)}}{\rightarrow N}$$

3. PER A

±1 count ± Trigger Error ± Time Base Error

4. TI A-B

±100 ns ±Time Base Errors ±Trigger Errors

5. PER AVG A

$$\pm \frac{100 \text{ ns}}{N} \pm \text{Time Base Error} \pm \frac{\text{Trigger Error}}{N}$$

6. TIA A-B

$$\pm \frac{100 \text{ ns}}{\sqrt{N}} \pm 10 \text{ ns} \pm \text{Time Base Errors} \pm \frac{\text{Trigger Errors}}{\sqrt{N}}$$

2-94. Dealing with One Count Error

2-95. There are several methods available for reducing the effect of one count error. The following considerations may be useful:

1. By selecting a longer gate time, the percentage error caused by the ±1 count gate uncertainty is decreased.

2. The accuracy of functions affected by ±1 count A depends upon the frequency of the input signal. As frequency increases, accuracy increases. As frequency decreases, accuracy decreases. With a higher frequency input, more counts will be made per gate time, and ±1 count error will become less significant. The percentage error is thereby reduced.

3. FREQ A and PER A functions can be used selectively to maximize accuracy of frequency measurements over the range of Channel A. The following can be drawn by this function comparison.

a. FREQ A provides the best measurement accuracy if the input signal is higher in frequency than the instrument time base oscillator (10 MHz).

b. PER A provides the best measurement accuracy if the input signal is lower in frequency than the instrument time base oscillator.

4. When using these guidelines, the operator must exercise discretion. In a high noise environment, or where a great deal of non-harmonic distortion might be expected, gate time errors due to improper triggering may be significant; FREQ A might be the better choice regardless of the input signal frequency.

2-96. Reducing Time Base Error

2-97. Some of the effects of crystal related time base errors can be reduced. If the temperature of the instrument environment is maintained at a constant value, temperature error is minimized. If tight control of the instrument environment fails to produce the accuracy desired, the time base crystal related error can be reduced through recalibration or by substituting a time base with smaller errors. This time base may either be one of the optional internal time bases described in Section 6, or an external 10 MHz reference connected to the instrument via the rear panel.

2-98. Trigger Error Considerations

2-99. Improperly triggered hysteresis levels can cause error when using any function. When using ratio or event timing functions, trigger errors produce gate time errors, resulting in inaccurate counts. Proper use of ATTENUATION and FILTER controls, along with other noise reduction techniques, will help solve this problem. In addition, the following considerations should be kept in mind:

1. Period measurements use Channel A for both START and STOP pulses; triggering errors are from one channel only. The period averaging function will reduce the effect of the triggering error by a factor of 1/N.

2. Time interval measurements use both Channel A and Channel B for the START and STOP pulses; the trigger error may arise from either or both channels. The averaging function will reduce the effect of the triggering error by a factor of $1/\sqrt{N}$.

3. In the ratio mode, the counts of Channel B trigger error increase as the frequency of the Channel A input signal increases.

4. A pulse input signal, with faster rise times, will exhibit less trigger error than a sine wave input.

2-100. Reducing Errors Due To Noise On The Input Signal

2-101. The following techniques may also be used to ensure noise rejection:

1. Use an oscilloscope to identify the presence of noise.

2. Use the ATTEN control to limit noise levels while maintaining sufficient signal levels for triggering.

3. Use an oscilloscope probe (X10) as the input cable when measuring high impedance circuits.

4. Use a low pass filter/attenuator. The front panel FILTER control can be utilized to attenuate signals above 100 kHz. Alternately, the Fluke Model Y7201 Filter/Attenuator, attached to the front panel input connector, can be used to suppress unwanted noise. This accesssory is described in Section 6 of this manual.

2-102. Summary

2-103. Some of the errors that affect accuracy are inherent and cannot be much improved without substituting different components (time base error). Accuracy can be improved by using the proper techniques (triggering error) or by selecting the correct function (PER A versus FREQ A). The accuracy of the event timing functions can be improved by using the appropriate averaging function. And, sometimes, the technique that decreases the effect of one error source increases the effect of another error source. Noise and distortion on the input signal or signals also affect the accuracy of measurement. The operator has to be aware of all facets of the error sources and exercise discretion in using the instrument to make precise measurements.

2-104. OPERATING DIRECTIONS

2-105. Operation of the 7260A for each function is described in the following paragraphs. Function capabilities, as well as useful operating hints, are also presented here.

2-106. Initial Procedure

2-107. The following procedural checks should be performed prior to using any of the function operating directions.

1. Check that the instrument has been connected to appropriate line power.

2. On the rear panel, ensure that the EXT-INT select switch is set to INT and that the AC POWER switch is ON.

3. Press power to ON (front panel).

4. Ensure adequate time for instrument warmup, especially if an optional oven time base is installed (typically 10 minutes).

2-108. Frequency Measurements (FREQ A)

2-109. Frequencies on Channel A from 0-125 MHz can be counted and directly displayed using this function. The

gate times available range from 0.1 ms through 10s in six decade steps selectable with the RESOLUTION control (respective markings of the 10 kHz through 0.1 Hz). Maximum inputs are listed in Section 1 (Specifications). Use the following procedure when making frequency measurements:

1. Set front panel controls as follows:

FUNCTION - FREQ A
RESOLUTION - as required, or AUTO
ATTENUATION - X100
TRIGGER LEVEL - PRESET
SEP/COM - SEP
FILTER - OUT

2. Connect the signal to be measured to the CHANNEL A input connector.

3. Adjust the ATTEN and TRIGGER LEVEL controls for a stable display.

4. Set the RESOLUTION control to obtain desired resolution of the displayed frequency. The OVFL annunciator will light if the display's capacity is exceeded.

NOTE

When dealing with low frequencies, period measurements yield greater accuracy.

2-110. Counts per Minute Measurements (CPM X100A)

2-111. The 7260A can be used as a tachometer to read out revolutions per minute. The input to Channel A in this function must be from a 100 pulse per revolution transducer. For transducers having other pulse per revolution rates, the 7260A readout can be converted to RPM with the formula:

$$\text{Correct RPM} = \frac{100 \text{ Displayed RPM}}{N}$$

Where N = the number of pulses per minute of the transducer.

1. Set front panel controls to:

FUNCTION - CPM X100A
SEP/COM - SEP
FILTER - OUT

2. Connect the transducer output to the CHANNEL A input terminal.

3. Adjust the ATTEN and TRIGGER LEVEL controls to ensure proper triggering.

NOTE

The output voltage from magnetic transducers will vary with speed of revolution. The ATTEN and TRIGGER LEVEL control settings may, in such cases, need to be changed. Alternately, a photo-electric transducer will provide an output level not dependent on frequency.

2-112. Frequency Measurements (Freq C)

2-113. Frequency measurements can be made above the range of FREQ A measurements using this optional function. Direct frequency measurements can be made in the range 50-520 MHz with the -310 Option installed. This option is discussed in detail in Section 6. Assuming the option is installed:

1. Set the Front Panel controls as follows:

FUNCTION - FREQ C
RESOLTUION - as required

2. Connect the signal to be measured to the Channel C input connector.

3. Change the settings of any controls as required to obtain a stable display.

4. Set the RESOLUTION control to obtain maximum resolution of the displayed frequency. The OVFL annunciator will illuminate if the display capacity is exceeded.

2-114. Ratio Measurement (RATIO A/B)

2-115. When using the RATIO A/B function, the instrument counts the frequency of input on Channel A and uses the frequency input on Channel B, instead of the reference frequency from the time base, to determine the length of gate time. The result is displayed without measurement units annunciation.

NOTE

The higher frequency must be input on Channel A.

2-116. The position of the Resolution control determines the number (N) of cycles of the Channel B input signal that must be used to determine gate time. The 10^0-10^5 scale is used. As the Resolution control also causes positioning of the decimal point, automatic averaging of the number of counts of A accumulated during N cycles of B will occur. Use the following procedure when making ratio measurements.

1. Set front panel controls as follows:

FUNCTION - RATIO A/B
RESOLUTION - set to optimize displayed resolution
SEP/COM - SEP
FILTER - OUT
ATTENUATION - X100, both channels
TRIGGER LEVEL -PRESET (both channels)

2. Connect the higher of the two frequencies to CHANNEL A input connector.

3. Connect the lower of the two frequencies to CHANNEL B input connector (0-2 MHz).

4. Adjust the ATTEN and TRIGGER LEVEL controls on both channels for proper triggering. (GATE LED flashing.) Gating is derived from the CHANNEL B signal when in the Ratio function; generally, the greater the level of the signal on CHANNEL B, the greater the accuracy of the Ratio measurement will be.

2-117. Period Measurements (PER A)

2-118. This function can be used to measure the period of an input signal with frequencies up to 2 MHz.

2-119. The period function provides a great improvement in both accuracy and resolution of measurements made on low frequency signals. To make period measurements, the instrument measures the time interval between two consecutive cycles of a repetitive signal; Channel A is used to generate start and stop pulses. The RESOLUTION control is used to specify the value of the least significant digit (100 ns-10 ms). Use the following procedure when making period measurements:

1. Set the front panel controls as follows:

FUNCTION - PER A
RESOLUTION - as required, or AUTO
SEP/COM - SEP
ATTENUATION - X100
TRIGGER LEVEL - PRESET

2. Connect the signal to be measured to the CHANNEL A input connector.

3. Adjust the ATTEN and TRIGGER LEVEL controls (Channel A) until a stable display is seen.

2-120. Period Averaging Measurements (PER AVG A)

2-121. Multiple periods of frequencies up to 2 MHz may be averaged to obtain greater resolution and accuracy than with Period measurements. For example, with a Period measurement of a 1 kHz signal, the display would read "1.0000 ms"; the maximum resolution of the Least Significant Digit is 100 ns. In Period Averaging, the same signal would be maximized at a display of "1000.0000 μs"; the resolution has increased to 1 ns. The number of periods measured, N, is selected in consecutive powers-of-ten. The total clock pulse count for all periods measured is accumulated; the decimal point is then shifted for averaging. The number (N) is selected by the Resolution control (range 10^0-10^5) for resolutions varying from 100 ns to 1 ps. As N increases, the average value approaches the correct value.

1. Set the front panel controls as follows:

FUNCTION - PER AVG A
RESOLUTION - as desired, or AUTO
SEP/COM - SEP
ATTENUATION - X100
TRIGGER LEVEL - PRESET

2. Connect the signal to be measured to the CHANNEL A input connector.

3. Adjust the ATTEN and TRIGGER LEVEL controls to ensure proper triggering.

2-122. Time Interval Measurements (TI A-B)

2-123. When the instrument makes time interval measurements, the START pulse is generated through Channel A and the STOP pulse is generated through Channel B. Use of the SEP/COM switch can either isolate the Channel A input from the Channel B input or connect Channel A input to both input amplifiers. With the switch in the COM position, events from the same source can be measured by Channel A and Channel B. With the switch in the SEP position, events from two sources can be measured on respective channels.

2-124. During time interval measurements, inconsistencies between channels may be noticeable. Hysteresis (sensitivity) levels will not be precisely the same for both Signal Conditioners. Accurate measurements of rise time, pulse width, etc., may be made through combined TRIGGER LEVEL and Slope control settings. Analog trigger level voltages (–1.5V to +1.5V) are available for either channel at the rear panel TRIGGER LEVEL connector.

2-125. There are several important specifications regarding the input signals for time interval measurements. The minimum time between the start level on Channel A and the stop level of Channel B can be less than 100 ns (the maximum display resolution). Times less than 100 ns will cause the 7260A to gate (GATE LED on), but the display will read zero. The pulse width for either

start or stop signal should be at least 50 ns. The time between the stop of one interval measurement and the start of the next is determined by the instrument's cycle rate (250 ms). The intervals measured are therefore samplings of the intervals available for measurement.

2-126. Triggering problems may appear in a number of ways when measuring time interval. An illuminated, but not flashing, GATE LED could mean that a proper stop signal is not being applied to Channel B. If the GATE LED is flashing, but there is no display, one or both of the input frequencies may be too high. Keep in mind that the 7260A is limited to a maximum of 5 MHz in Time Interval mode. Ringing on the input signal may be lessened by increasing the ATTENUATION or by using an appropriate termination.

NOTE

The time interval function should not be used when period measurements are to be made.

1. Set front panel controls as follows:

FUNCTION - TI A-B
RESOLUTION - as desired, or AUTO
SEP/COM - SEP if the start and stop signals are from separate sources. COM if the start and stop signals are from the same source.

CHANNEL A SLOPE - set to + for triggering on the positive slope of the input, or to – for negative slope.

CHANNEL A ATTENUATION -X100
CHANNEL B SLOPE - + or – as required
CHANNEL B ATTENUATION - X100

2. For separate input signals, connect the start signal to CHANNEL A input connector and the stop signal to CHANNEL B. For common inputs, connect the signal to Channel A.

3. Reposition ATTENUATION on the CHANNEL A input until the GATE LED comes on. This action ensures proper triggering by the start signal.

4. Reposition ATTENUATION on the CHANNEL B input until the GATE LED begins to flash, ensuring proper stop triggering.

2-127. Time Interval Averaging Measurements (TIA A-B)

2-128. Multiple time intervals can be averaged to obtain greater resolution and accuracy than with Time Interval measurements. Use the following procedure when making Time Interval Averaging measurements:

1. Set the Front Panel controls as follows:

FUNCTION - TIA A-B
ATTENUATION - X100
TRIGGER LEVEL - PRESET

2. Set all other instrument controls as necessary for the application at hand.

3. For inputs from separate sources, connect the start signal to Channel A input terminal and set the SEP/COM switch to the SEP position. For inputs from a single source, connect the signals to the Channel A input terminal and set the SEP/COM switch to the COM position.

4. Adjust the instrument controls as described in the Operating Notes earlier in this section to insure stable display triggering at the proper points.

2-129. Totalizing Measurements (TOT A·B)

2-130. In the totalize mode, the 7260A can be used to continuously count and display the number of events occurring on Channel A during each event on Channel B. Only a reset will reinitialize the count. Use the following procedure for totalize measurements:

1. Set front panel controls as follows:

FUNCTION - TOT A
RESOLUTION - not used
SEP/COM - SEP
ATTENUATION -X100 (both channels)
TRIGGER LEVEL - PRESET (both channels)

2. Connect signal to be totalized to CHANNEL A input connector.

3. Connect gating signal to Channel B.

4. Adjust the ATTEN and TRIGGER LEVEL controls (Channel A) to ensure proper triggering.

5. Reposition Channel A ATTENUATION until an updating display is seen during the gate.

NOTE

Should a continuous totalized count of Channel A be desired, connect a DC source (100 mV rms) to Channel B. Alternately, Channel B TRIGGER LEVEL control can be adjusted to enable a continuous count.

2-131. Self Check (CHK)

2-132. The self-check function can be used to verify the digital operation of the 7260A. Each setting of the RESOLUTION control will provide a predictable display of the 10 MHz reference frequency. To self-check the 7260A, use the following procedure:

1. Press the power switch to ON.

2. Set the FUNCTION control to CHK.

3. Momentarily press the RESET control; the display should read "88888888" while RESET is depressed.

4. Set the RESOLUTION control to AUTO; the display should read "10000.00 kHz".

5. Verify correct display for each of the remaining six RESOLUTION settings as defined in Table 2-4.

Table 2-4. CHK Function Display

RESOLUTION SWITCH SETTING	DISPLAY
0.1 Hz	*0000.0000 kHz
1 Hz	10000.000 kHz
10 Hz	10000.00 kHz
100 Hz	10.0000 MHz
1 kHz	10.000 MHz
10 kHz	10.00 MHz
* Overflow annunciator should be illuminated.	

Section 3
Theory of Operation

3-1. INTRODUCTION

3-2. The 7260A Universal Counter/Timer will be explained on two levels in this section. FUNCTIONAL DESCRIPTION, referenced to the functional block diagram Figure 3-1, deals with each of the more common 7260A functions. In addition, each mode of operation will be separately described and illustrated. CIRCUIT DESCRIPTION will then provide a more specific accounting of 7260A operation; various figures present simplified schematic diagrams of these descriptions. Refer to Section 8 of this manual for detailed schematic diagrams and a list of mnemonics.

3-3. FUNCTIONAL DESCRIPTION

3-4. The 7260A Universal Counter/Timer is capable of the following measurements: frequency, period and period average, counts per minute, time interval, time interval average, ratio, totalize A gated by B, and self check. The optional Channel C allows frequency measurement up to 520 MHz. The functional description of the instrument will consist of a basic block description followed by a description of each instrument function.

3-5. Basic Block Diagram

3-6. The major functional areas of the instrument are shown as basic blocks in Figure 3-1. Each block performs the following operations:

1. Control Logic: This block provides logic and timing functions for the 7260A. The positions of the RESOLUTION and FUNCTION controls are decoded. The decoded commands signal the control logic to perform several operations: illuminate the proper decimal point and unit's annunciator, enable the correct Function and Resolution Logic, and produce one of six decade divided gating frequencies.

2. Signal Conditioners: These blocks condition the input signal for compatibility with other circuitry within the counter. A Signal Conditioner will provide a pulse train output, with each pulse corresponding to one cycle or event of the input signal.

3. Time Base: Depending on the FUNCTION selected, the Time Base (with dividers) supplies 10 MHz, 1 MHz, or 1/6 MHz. These three frequencies are derived from one of the available 10 MHz frequency standards or through the EXT 10 MHz input jack on the 7260A's rear panel.

4. Frequency C Control: When a Channel C option is installed, this block controls frequency counting using circuits on both the Option PCB and the 7260A Main PCB.

5. Power Supply: This block utilizes conventional power supply and regulation techniques to supply outputs of +5V to all digital circuitry, –5V to the Signal Conditioners, +12V and –12V to control circuitry. When an optional oven time base is installed, oven voltage (+5V) remains energized when the front panel power switch is placed in STBY. When the Rear Panel REF switch is set to EXT, oven voltage is disconnected.

6. Main Gate: When enabled, the Main Gate passes pulses from the Clock Select functional block to Count and Display. Gate Select (enable) and Clock Select inputs to the Main Gate vary by function, as defined in Table 3-1.

7. Clock Select: This block routes signals to the Main Gate clock input for count and display. The Clock Select block is under direct control of signals from Control Logic.

8. Gate Select: This function enables the Main Gate for a period determined by Control Logic.

9. Count: The Count function utilizes eight counter decades and latches. An internal oscillator sequences through count, latch, and output periods to provide BCD and strobe outputs to Display.

10. Display: This function provides BCD to seven segment decoding for display of the count. Decimal points and measurement units are determined by Control Logic.

11. Time Interval Flip-Flop: This function derives the start pulse from Channel A and the stop pulse from Channel B for enabling of the Main Gate.

12. Time Interval Average Control: This block receives the output pulse from the Time Interval F/F that enables the Main Gate. At the trailing edge of the Time Interval F/F pulse, this circuit will generate two pulses: a 2 μsec pulse to increase the Control Logic counter by one and a 4 μsec Reset pulse to Reset both the START and STOP portions of the Time Interval F/F.

13. Time Interval Holdoff: This circuit is an analog timer that prevents Channel B from generating the STOP pulse during TI or TIA functions for a preset length of time after the START pulse. The length of time is selected by the Front Panel TI Holdoff control.

14. CPM Control: When in the Counts Per Minute function, this functional block overrides RESOLUTION settings and routes the 1/6 MHz Time Base to Control Logic; a fixed gate time of 600 ms is established. In addition, this block disables decimal point and measurement unit outputs to the Display.

15. Function Decode: Function line settings from either the front panel or the remote interface are decoded for application to Control Logic and various other signal control and routing circuits.

16. Resolution Decode: Data selection circuit adapts resolution line settings to Control Logic inputs. Special circuits also decode a setting on the lowest resolution for use in Time Interval Average, Period Average or Ratio measurements.

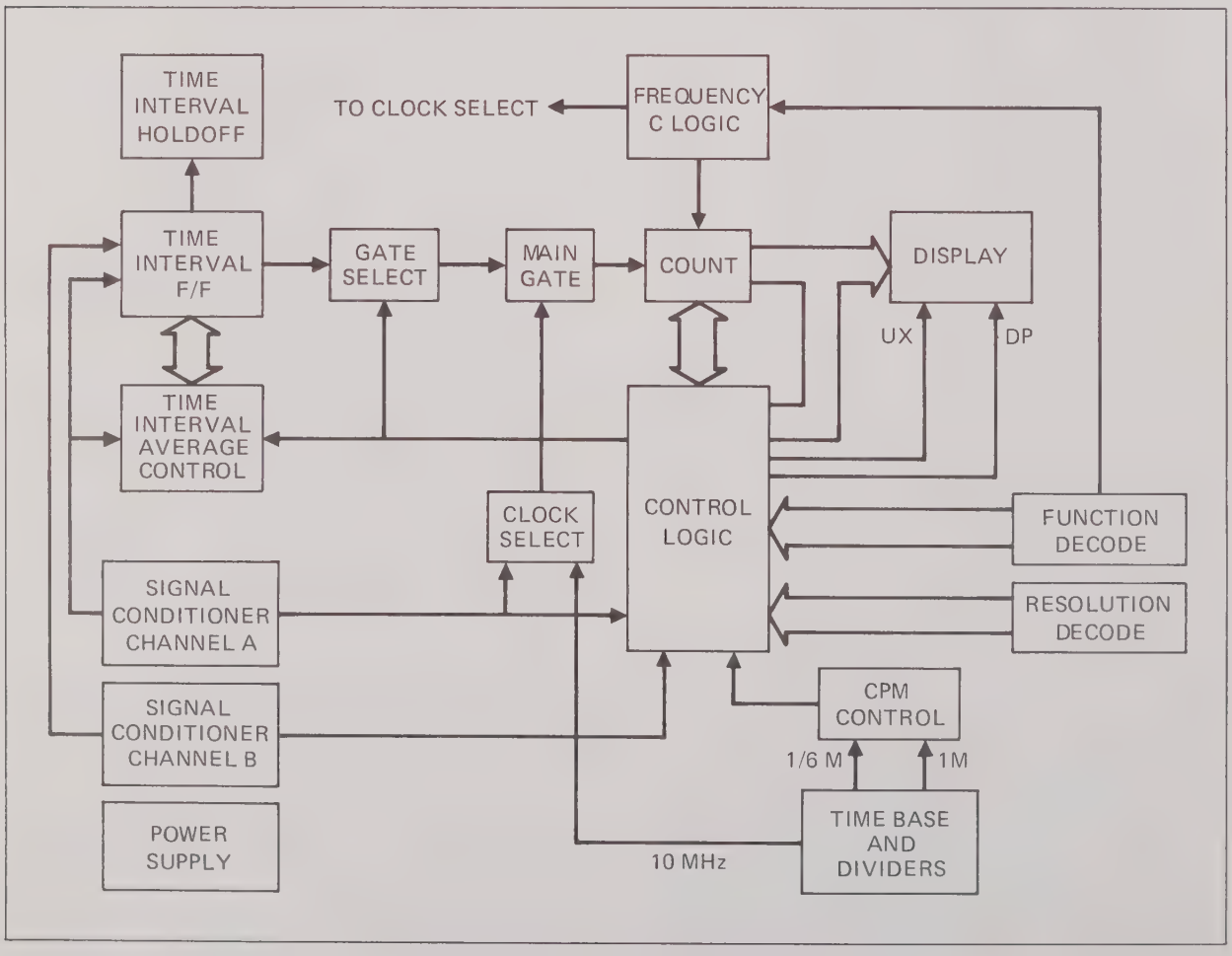


Figure 3-1. Functional Block Diagram

Table 3-1. Main Gate Inputs

FUNCTION	CLOCK SOURCE	GATE SOURCE
FREQ A	Channel A Input	Decade Divided Time Base from Control Logic
CPM X100A	Channel A Input	600 msec from Control Logic
FREQ C	Channel C first decade carry	Decade Divided Time Base from Control Logic
RATIO A/B	Channel A Input	Channel B Input
PER A	Decade Divided Time Base from Control Logic	Channel A Input Divided by Control Logic
PER AVG A	10 MHz Time Base	Channel A Input Divided by Control Logic
TI A-B	Decade Divided Time Base from Control Logic	Determined by Channel A start and Channel B stop
TIA A-B	10 MHz Time Base	Determined by Channel A start and Channel B stop
TOT A·B	Channel A Input gated by B input	Constant enable from Control Logic
CHK	10 MHz Time Base	Decade Divided 10 MHz Time Base

3-7. Frequency (FREQ A) Measurements

3-8. When used in this mode, the 7260A will accumulate and display cycles of an input frequency for a specified length of time. This interval, known as the gate time, may be 0.1 ms, 1 ms, 10 ms, 0.1s, 1.0s, or 10s. The positioning of the decimal point, as determined by the resolution setting, will translate the displayed cycle count to units of kHz or MHz. For example, an input frequency of 2.3 MHz being measured on the 100 Hz RESOLUTION setting would yield a display of (2 . 3 0 0 0 MHz). The gate time, in this case 10 ms, would allow 23,000 cycles of the input frequency to be counted; the displayed number without decimal point will always equal the actual number of cycles counted during the gate time. This count would then be displayed as the input frequency by repositioning of the decimal point and illumination of the MHz units annunciator.

3-9. Frequency (FREQ A) mode is illustrated on an operational function level in Figure 3-2. Control Logic determines most other function operation. In particular, the 1 MHz reference is decade divided by Control Logic to provide the six gate times for Gate Select. Clock Select is set by Control Logic signals to route the Channel A input to the Main Gate. With the Main Gate enabled by Gate Select, the Channel A frequency will be transferred to Count and Display.

3-10. Counts per Minute (CPM X100A) Measurement

3-11. The 7260A will display revolutions per minute (RPM) when used in this mode. A 100 count per revolution transducer must be used as the input to Channel A to obtain a correct direct readout. The front panel RESOLUTION control will have no effect in this mode; the instrument will display a fixed resolution of 100 CPM. There will be no decimal point or units annunciator activated.

3-12. Counts per Minute measurement is shown on a functional level in Figure 3-3. Time Base Dividers provide a 1/6 MHz reference frequency to CPM Logic. CPM Logic performs three functions. First, the 1/6 MHz reference is routed to Program Control Logic. Secondly, CPM Logic provides a fixed range setting. Finally, decimal point placement and units annunciators are disabled. Control Logic decade divides the 1/6 MHz reference to 1 2/3 Hz: Gate Select thereby enables the Main Gate for 600 ms. Clock Select routes the input on Channel A to the Main Gate to be fed to Count and Display.

3-13. Frequency C (FREQ C) Measurement

3-14. The optional Frequency C measurement function, while the same as Frequency A, utilizes a separate Channel C input terminal and signal conditioner. The -310 Option allows frequency measurements over the range of 50-520 MHz. This option is discussed in detail in Section 6.

3-15. Ratio (RATIO A/B) Measurement

3-16. Ratio measurement yields a numeric display, without measurement units, of the Channel A signal (0 - 125 MHz) divided by the Channel B signal (0 - 2 MHz). Refer to Figure 3-4 for the following block description. The Channel A input, always the higher frequency, is routed to the Main Gate through Clock Select. The Channel B input is decade divided within Control Logic. Depending on the RESOLUTION setting, one of six periods then enables the Main Gate through Gate Select.

The number of pulses of the Channel A Signal counted during the main gate enable is then displayed without measurement unit. This displayed number is the cycle count of the Channel A signal during one period of the divided Channel B signal. With decimal point placement, this number yields the ratio between the two inputs. For example, with 5 MHz on Channel A, 500 kHz on Channel B and a RESOLUTION setting of 10^1, the Main Gate will be enabled for 20 μs. During this time, 100 cycles of the Channel A frequency will be counted, and the display will yield a reading of "10.0".

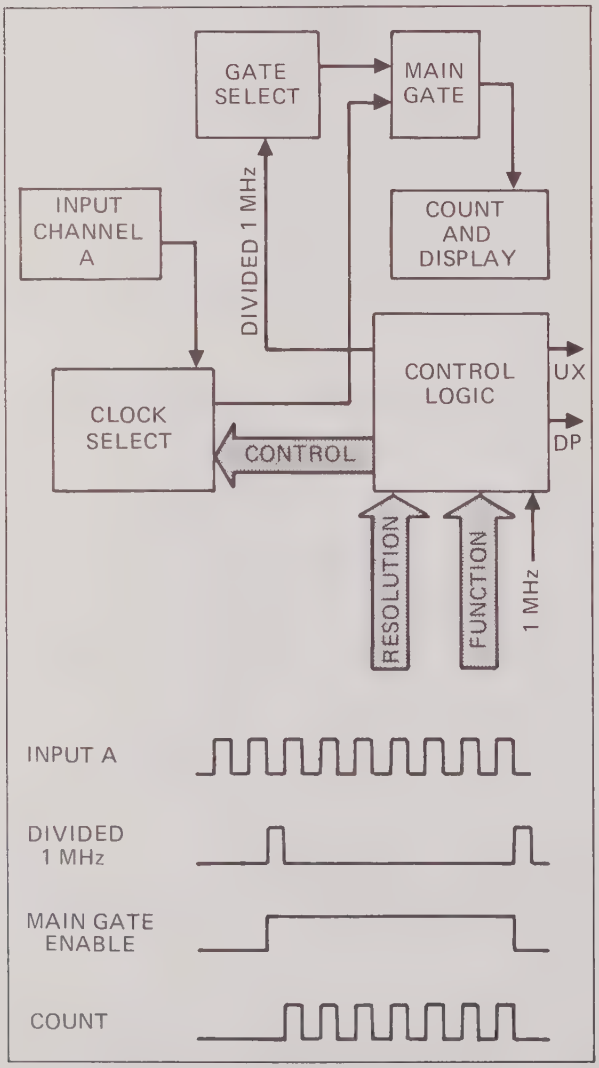


Figure 3-2. Frequency Measurements

3-17. Period (PER A) Measurements

3-18. The period of the Channel A input signal is measured by counting a reference frequency for an interval determined by the input signal. Depending on the RESOLUTION setting, the 7260A will count a reference frequency of 10 MHz, 1 MHz, 100 kHz, 10 kHz, 1 kHz or 100 Hz. The display will then show the total count of the reference frequency for the period of one cycle of the input frequency. With repositioning of the decimal point and illumination of the "μsec", "msec" or "sec" units annunciator, this count will identify the period of one Channel A input cycle. For example, with a Channel A input frequency of 400 kHz set for PER A measurement with 100 ns RESOLUTION, the 7260A will count a 10 MHz reference frequency for 2.5 μs. A count of 25 will be accumulated and displayed. The RESOLUTION setting will also specify the decimal point and measurement unit for the display; a reading of (x x 0 . 0 0 2 5 ms) will be displayed. The total count of the reference frequency is thereby displayed.

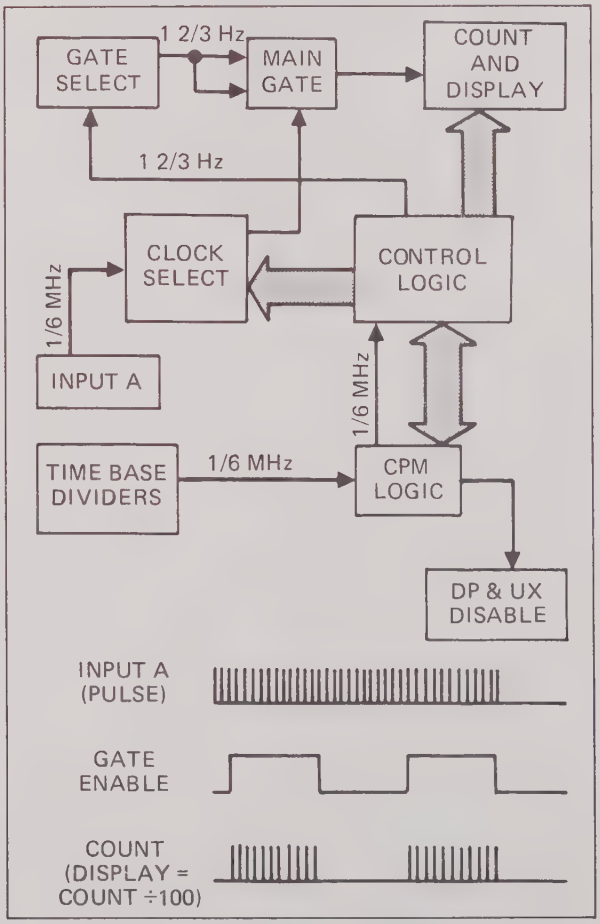


Figure 3-3. Counts Per Minute Measurements

3-19. Period measurement is functionally illustrated in Figure 3-5. Control Logic determines most other function operation. Gate Select will be controlled by the Channel A input frequency, routed through Control Logic. Clock Select will be derived from the 10 MHz Time Base; either the 10 MHz or one of five decade divided frequencies from the Control Logic will be used to clock the Main Gate. This clock will be fed to Count and Display whenever the Main Gate is enabled by Gate Select.

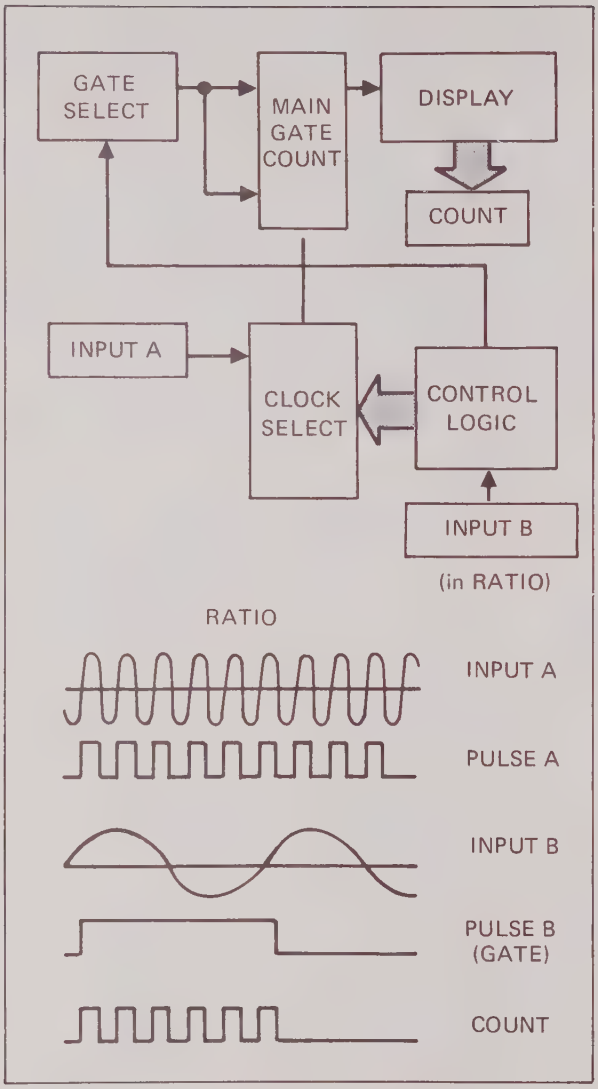


Figure 3-4. Ratio Measurements

3-20. Period Averaging (PER AVG A) Measurement

3-21. During period averaging measurements, the 7260A will count a reference frequency for an interval equal to multiple cycles of the Channel A input frequency. The Front Panel RESOLUTION control will determine the number of input cycles during which the reference frequency is counted (10^0 - 10^5 input cycles in decade steps). The reference frequency will now be the 10 MHz time base only. As in period measurements, the decimal point and units annunciator will be utilized to display the average elapsed time for one period of the Channel A input frequency. As an example, a 400 kHz Channel A input signal could be measured with the RESOLUTION control set to "10^3". The 10 MHz reference frequency will now be counted for 1000 cycles of the input signal: 25,000 counts will be displayed. The decimal point and units annunciator will specify the display to read (2.5000 μs). The display's resolution is thereby greatly enhanced. A resolution of 100 ps is shown in Period Average, whereas the same signal exhibited only 100 ns resolution in the Period measurement example.

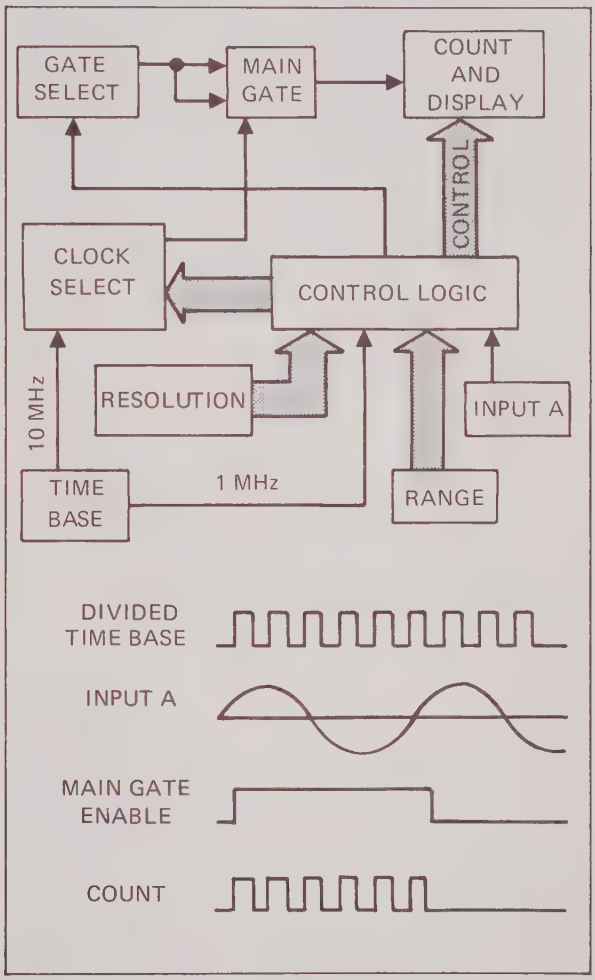


Figure 3-5. Period Measurements

3-22. An illustrated functional approach to Period Average measurement is provided in Figure 3-6. Control Logic enables Clock Select to apply the 10 MHz to the Main Gate. The input frequency (Input A) is decade divided by Control Logic; depending on the RESOLUTION setting, the Channel A frequency or one of five derived frequencies is applied to Gate Select. The Main Gate is thereby enabled for an interval equal to 10^0 to 10^5 cycles of the Channel A input. When enabled, the Main Gate feeds the 10 MHz reference to Count and Display. Control Logic then determines display update, decimal point placement and units annunciation.

3-23. Time Interval (TI A-B)

3-24. For time interval measurements, the 7260A will display counts of a scaled reference frequency for a period

whose start is determined by the Channel A input signal and whose stop is determined by the Channel B signal. Refer to Figure 3-7 during the following block diagram discussion. One of six reference frequencies is selected by the RESOLUTION Control for routing through Clock Select to the Main Gate. These frequencies are the 10 MHz time base and five derived frequencies (1 MHz-100 Hz) from Control Logic. Gate Select is held enabled by Control Logic, allowing the Time Interval Flip-Flop to control the Main Gate. Depending on the Slope Control setting, a positive or negative going Channel A input will now enable the Main Gate to pass the reference frequency. Under similar control, the Channel B signal will disable the Main Gate. The accumulated counts of the reference frequency between A and B inputs are displayed as in Period measurements.

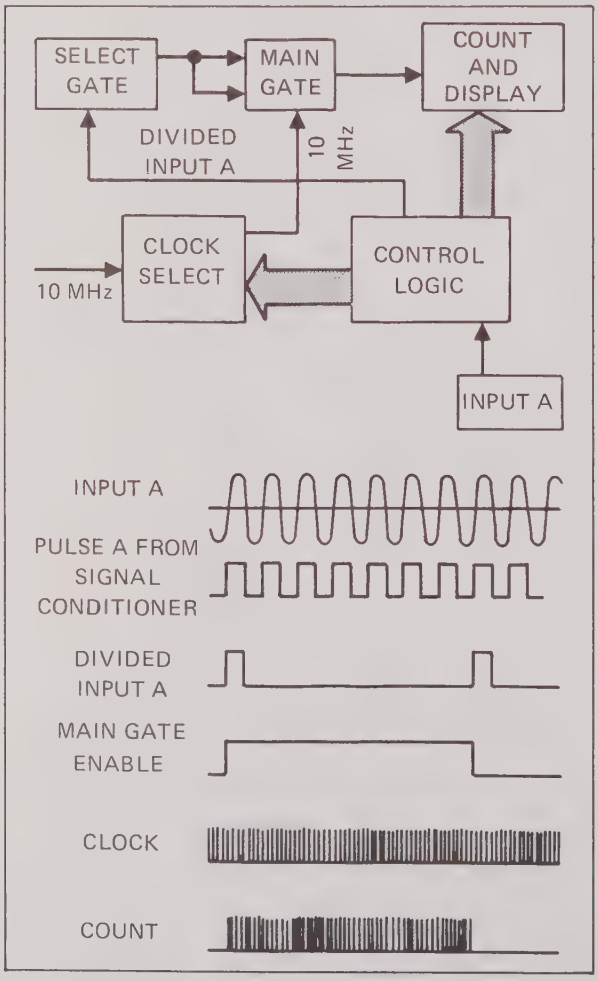


Figure 3-6. Period Averaging Measurements

3-25. Time Interval Average (TIA A-B) Measurements

3-26. For time interval average measurements, the 7260A will display the average number of counts of the 10 MHz clock that occur during each period of a repetitive signal. To find this average number, the counts that occur during N periods are divided by N. The Front Panel RESOLUTION control will determine N, the number of time intervals averaged (10^0 - 10^5 intervals). The decimal point and units annunciators will be utilized to display the average time interval measured. For example: Two input frequencies with a time interval of 1.5 μsec and a repetition rate of 100 kHz are measured with the RESOLUTION control in the 10^2 position. The instrument will count 10 cycles of clock frequency during each time interval for 100 intervals. The total count will be 1000. The display will show 1.000 μsec. Using the resolution formula in Table 1-2, resolution possible on this range using the TIA function is 10 ns maximum. Resolution of the same range in time interval function is only 10 μsec.

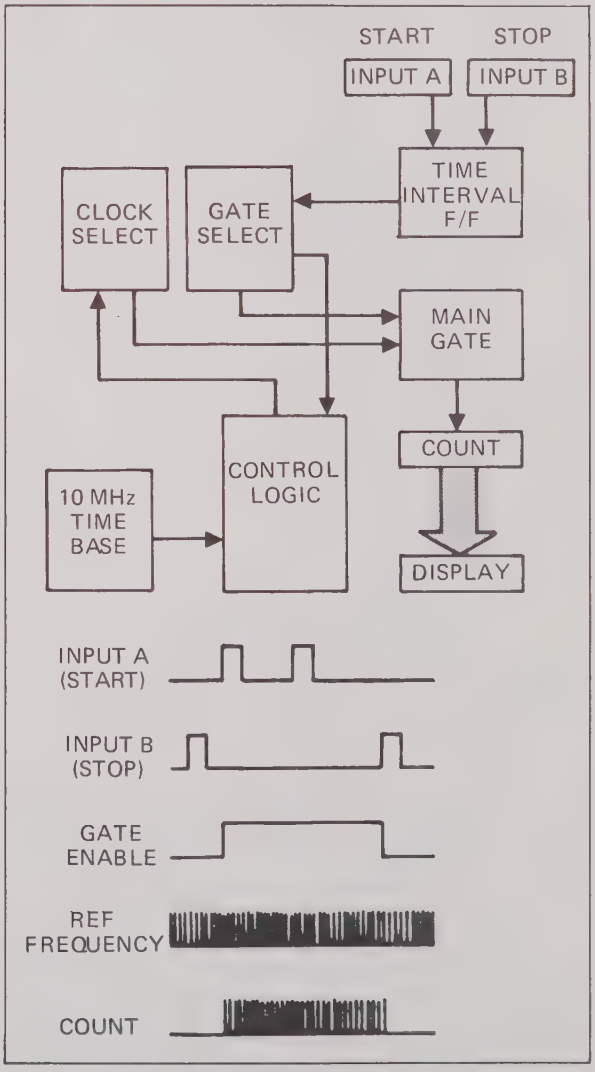


Figure 3-7. Time Interval Measurements

3-27. Figure 3-8 is a simplified diagram of the time interval average function. At the beginning of a

measurement cycle, Control Logic enables the Gate Select circuitry so that the Time Interval F/F controls the Main Gate. Control Logic also routes the 10 MHz signal to the Main Gate clock input.

3-28. As in time interval measurements, the START pulse is generated through Channel A. This pulse will cause the Time Interval F/F to open the Main Gate. The Count circuitry begins to accumulate pulses of the 10 MHz signal. At some later time, the STOP pulse causes the Time Interval F/F to close the Main Gate. Count now holds the total number of cycles of the 10 MHz signal that occurred during the time interval. This measurement sub-cycle will continue until Control Logic removes the enable signal from the Gate Select circuitry.

3-29. The signal from the Time Interval F/F that opened and closed the Main Gate also goes to the Time Interval Average Control circuit. The trailing edge of the signal from the Time Interval Average Control circuit triggers two pulses: a 2 μsec pulse to the Control Logic clock input and a 4 μsec Reset pulse to the Channel A and Channel B Input Circuitry. The 2 μsec pulse increments a Control Logic timer once for each time interval measured. After N (the number of time intervals selected by the RESOLUTION control) interval counts have been accumulated in the counter, the Control Logic causes the average time interval value to be displayed. This time interval value is the total accumulated count of clock pulses that occurred during all of the time intervals measured, divided by the number of time intervals measured. Since the number of time intervals is always a power-of-ten, the division is accomplished by moving the decimal point position. The 4 μsec pulse from the Time Interval Average Control circuit holds the STOP and START gates off; the time intervals measured are not consecutive.

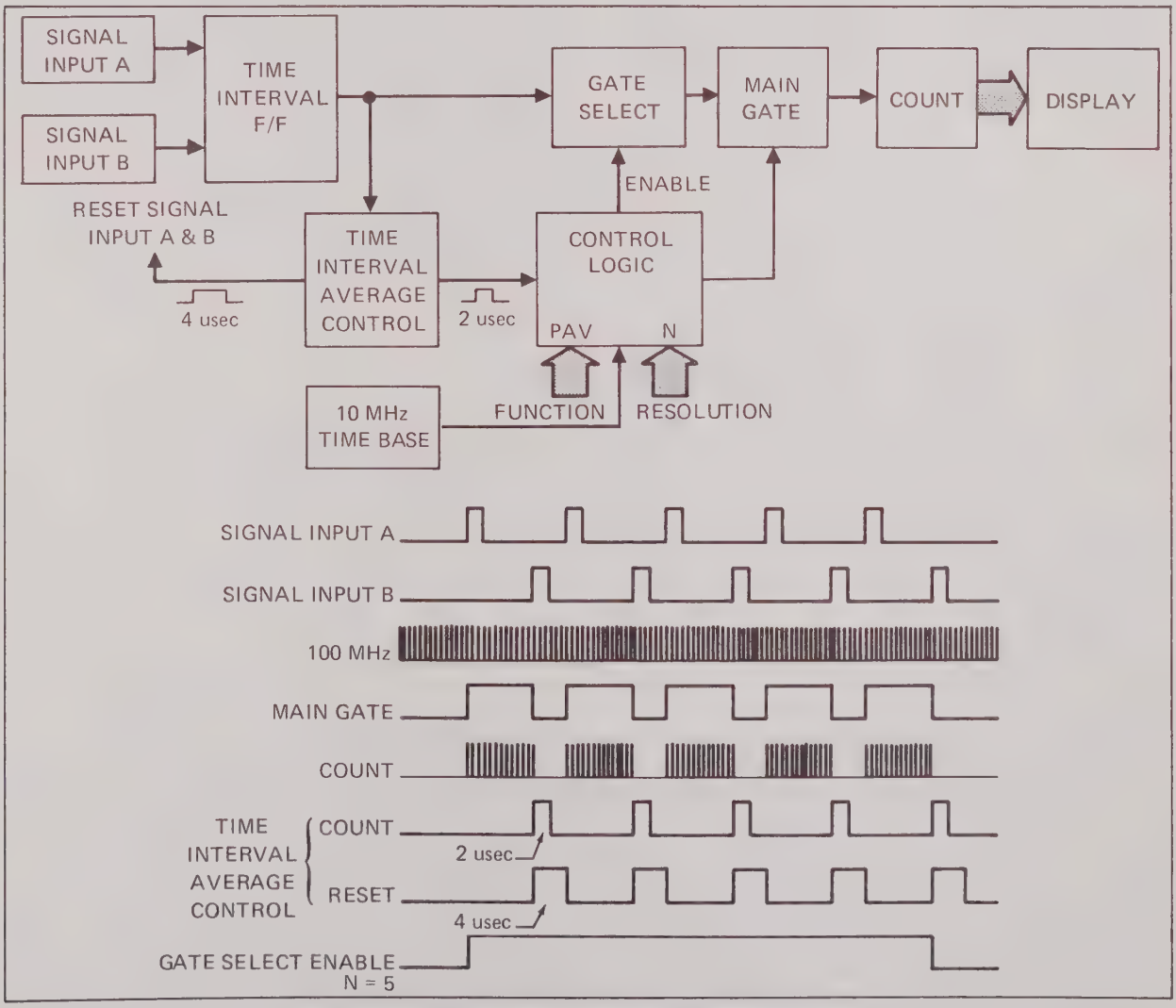


Figure 3-8. Time Interval Average A • B Measurements

3-30. Totalize A Gated by B (TOT A·B) Measurement

3-31. During totalize measurements, the outputs of the Channel A and Channel B signal conditioners are ANDed then counted. The number displayed represents a continuing total number of triggering events that occur on Channel A when an event occurs on Channel B. The 7260A will restart this count only when a reset is applied. No measurement units or decimal points are used during totalize measurements. Refer to Figure 3-9 for the following functional block description. A constant Main Gate enable is supplied from Control Logic through Gate Select. Channel A input pulses clock the Main Gate and are displayed to a maximum count of "99999999".

3-32. Self Check (CHK) Measurement

3-33. In the self check mode, the 10 MHz reference frequency is used as a dynamic verification of counter digital circuitry operation. Neither input and signal conditioning circuitry nor time base accuracy can be checked in this function. Each setting of the RESOLUTION control yields a predetermined display readout as defined in Table 3-2. Refer to Figure 3-10 during the following block description. Control Logic disables inputs from the Channel A Signal Conditioner while providing digital control for Clock Select, Gate Select, Count and Display functional blocks. Clock Select routes 10 MHz from the Time Base to the Main Gate. Depending on the RESOLUTION setting, Gate Select enables the Main Gate for a duration derived from the 10 MHz reference in Control Logic. The 10 MHz Clock Select frequency is thus counted and displayed for gate times of 0.1 ms to 10s. Overflow indication will occur at the 1 Hz and 0.1 Hz settings.

3-34. CIRCUIT ANALYSIS

3-35. The following descriptions detail key circuit operation in the 7260A. Circuit descriptions for options are presented in Section 6 of this manual. It is recommended that the FUNCTIONAL DESCRIPTION be read first for an overall understanding of the instrument. The simplified schematic diagrams presented here are referenced in the applicable paragraphs. Complete schematic diagrams and mnemonic definitions will be found in Section 8.

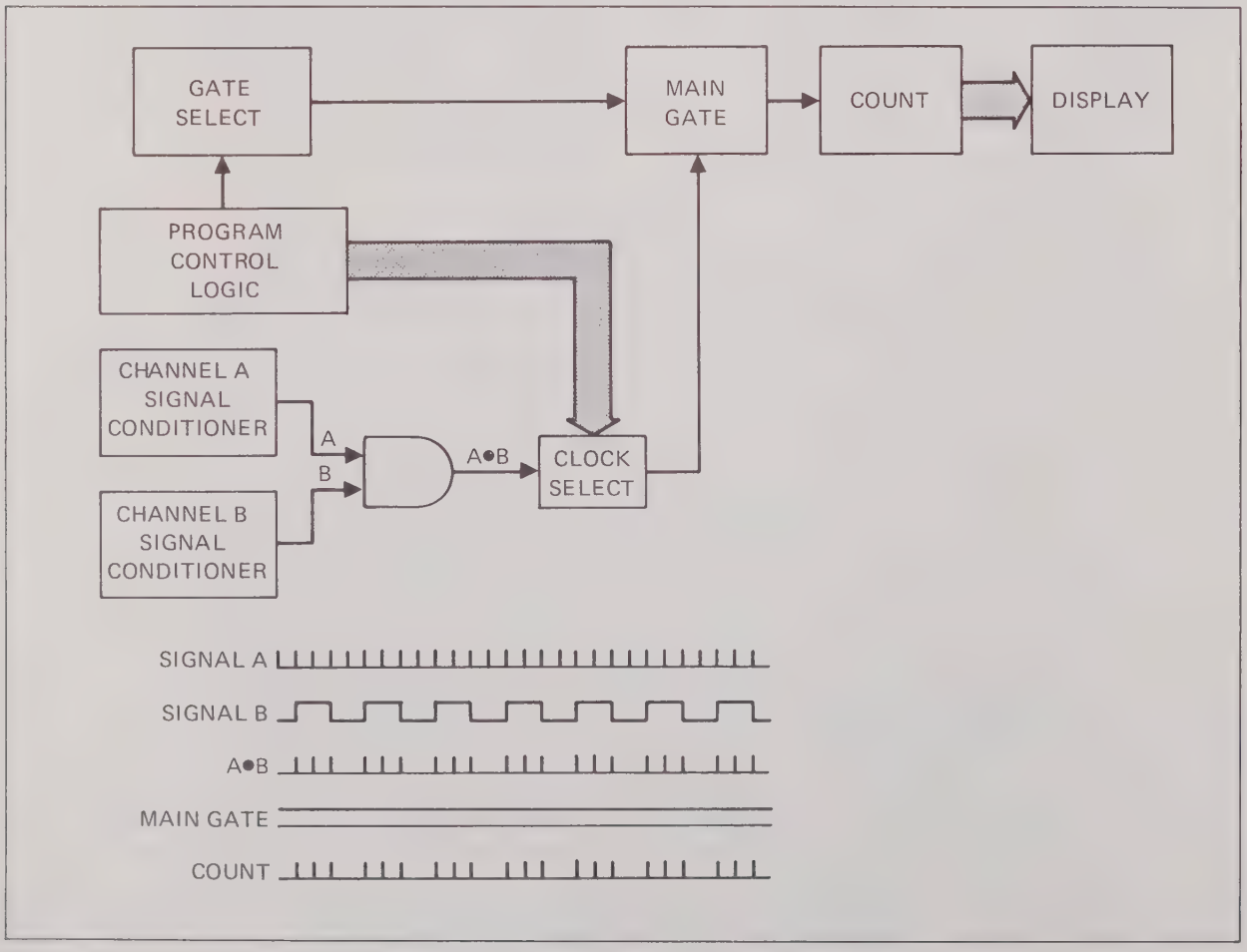


Figure 3-9. Totalize A Gated by B Measurements

Table 3-2. Display Readout in Self-Check Mode

RESOLUTION	DIGIT DISPLAY	MEASUREMENT UNIT
10 kHz	10.00	MHz
1 kHz	10.000	MHz
100 Hz	10.0000	MHz
10 Hz	10000.00	kHz
1 Hz	10000.000	kHz
0.1 Hz	0000.0000	kHz (OVFL)
AUTO	10000.00	kHz

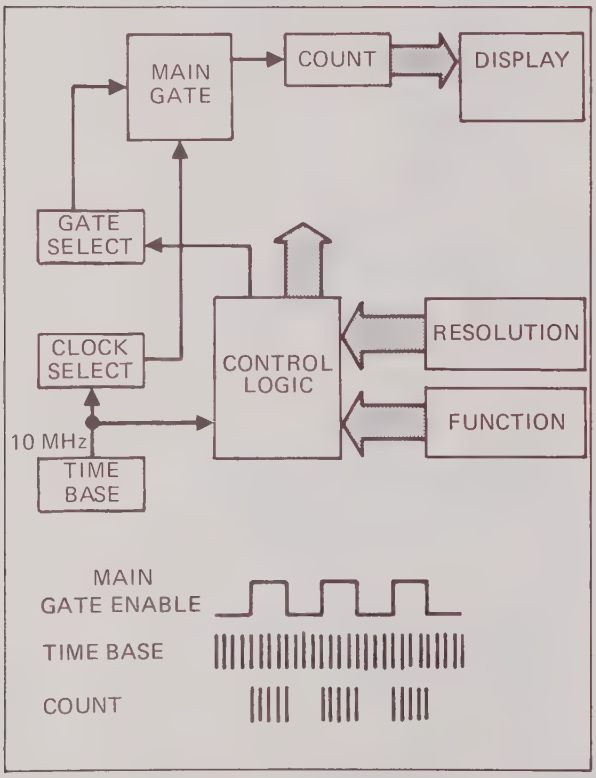


Figure 3-10. Self-Check

3-36. Power Supply

3-37. The 7260A Power Supply utilizes standard ac to dc rectifying, filtering and regulating circuitry to provide regulated outputs of –5V, +5V, –12V, and +12V. With the Battery Option (-010) installed, unregulated inputs of –5V, +5V, –12V and +12V are supplied to the regulators. Accomodation to line voltages of 100V, 120V, 220V, OR 240V is achieved through positioning of S4 and S5 in the power transformer's primary. The –5V is supplied by tracking regulator U15; which tracks the +5 volt supply. The Rear Panel ON-OFF switch removes primary power from the supply transformer. The Front Panel ON/STBY switch (S3) disconnects the regulated voltages from 7260A circuitry; the STBY position will maintain +5V to any installed oven time base. Protection diodes CR7 and CR8 prevent damage to the power supply should –12V or +12V lines become shorted.

3-38. Time Base

3-39. The 10 MHz reference is supplied by an internal free air time base, an optional internal time base, or by an external time base applied through the rear panel connector. Schmitt trigger U37-2 provides a shaped output from the time base in use. This 10 MHz reference may be used directly as the Main Gate clocking signal when Control Logic pins EH and CO are high. The 10 MHz signal is also divided to provide three additional references. First, 1 MHz is produced by decade divider U19-13. Next, U2-14 (divide by six) produces 1/6 MHz from the 1 MHz signal. Finally, decade divider U19-3 provides 100 kHz from the 1 MHz signal. The 1 MHz and 1/6 MHz signals are applied to Time Base Selector U1-8 for application to Control Logic input CI; 1/6 MHz is used only in Counts per Minute mode. The 100 kHz signal is used with the Gate Time Synchronizer (U4-6) and Time Interval Average circuitry.

3-40. Input Circuitry

3-41. Identical input circuitry is utilized for Channel A and Channel B. For either Channel, the input signal is amplified, filtered, and shaped to provide an output at ECL logic levels. Figure 3-11 illustrates input circuitry for either channel. Each input is fuse protected (250 mA) and may be either AC or DC coupled to the three position attenuator. The attenuator provides three attenuation factors: X1 X10 and X100. At this point the Channel A and Channel B input circuits may be tied together through the SEP/COM switch.

3-42. Within the Signal Conditioner, the signal passes two clamping diodes and an input buffer prior to entering the Preamplifier IC. The Preamplifier IC contains an amplifier, a Schmitt Trigger for signal shaping, and an ECL driver. Trigger Level is selected by changing the negative input to the Input amplifier. If the Front Panel TRIGGER LEVEL control is in the PRESET position, a fixed resistance is selected to set the level at 0V. This fixed voltage can be adjusted during the calibration adjustments presented in Section 4. Positioning of the Front Panel TRIGGER LEVEL control off PRESET varies the offset of the amplifier continuously between +1.5V and –1.5V. The hysteresis window of the Schmitt trigger is permanently selected by the hysteresis resistor located on the Main PCB (R4 for Channel A, R3 for Channel B). The bandpass of the Input Amplifier can be reduced from 0-125 MHz to 0-100 kHz by placing the FILTER control IN. The Q and $\overline{Q}$ ECL outputs are routed to the Main PCB (for signal processing) and to the Front Panel (to drive the ± trigger status indicators).

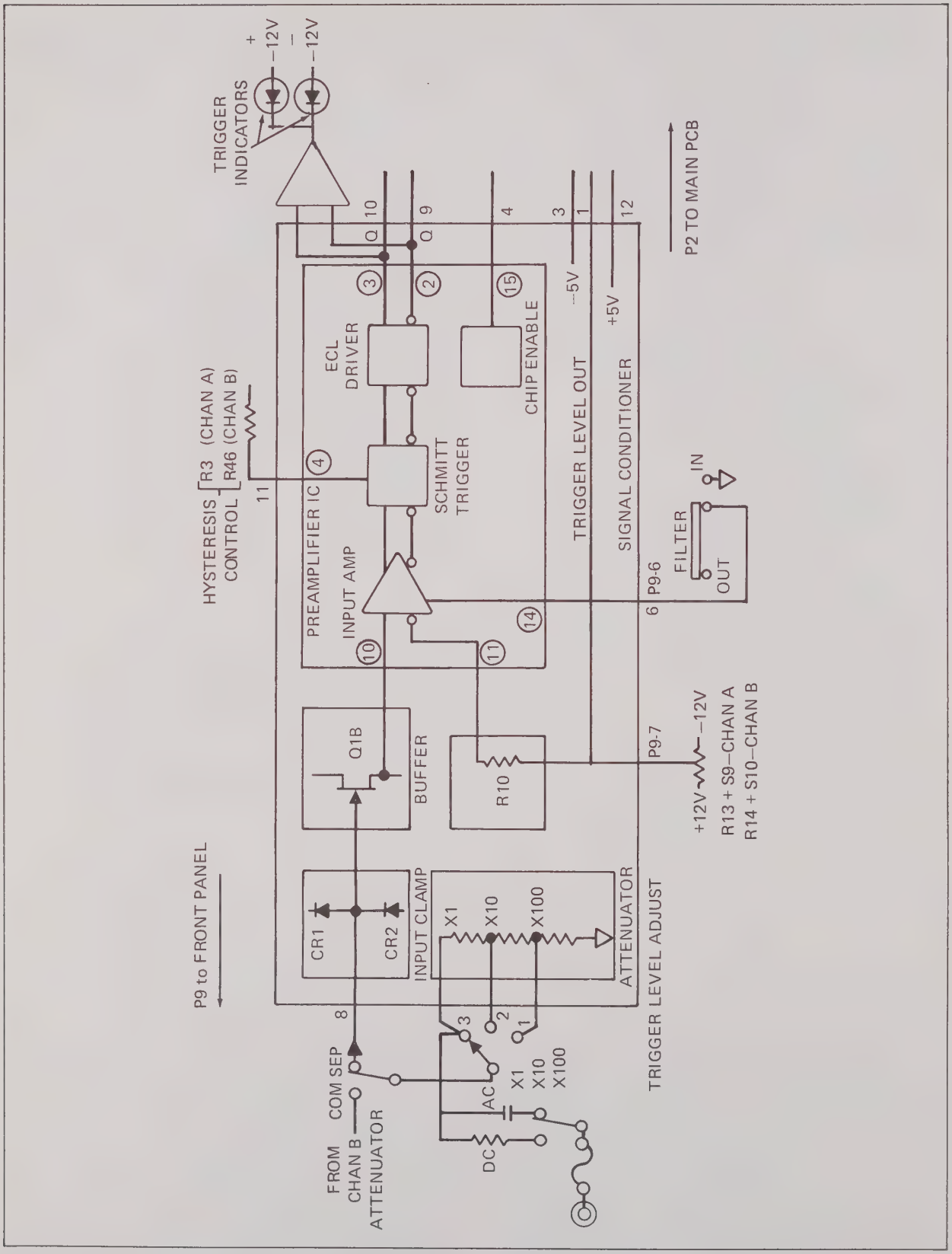


Figure 3-11. Input Circuitry

3-43. Function Logic

3-44. Instrument function selection is determined by data lines F1, F2, F4 and F8. Logic levels for the BCD coding on these lines emanate from either the front panel FUNCTION control (local) or through the optional Data Input/Output Unit (remote). Tri-state buffer U39, under control of the $\overline{\text{REM}}$ line, selects local or remote function inputs. Most function related operations, such as gate selection and clock selection, will be determined within Control Logic U12. Function inputs to U12 are a M1, M2 and M3. Other function dependent circuitry is controlled by decoded outputs from a 256 bit ROM - U38. All function commands, whether to U12 or other circuits, are decoded by this ROM. Function decoding ROM U38 is provided logic encoding on lines F1, F2, F4 and F8, along with an input from range zero decoder U27. Table 3-3 defines U38 inputs and outputs for each function. Outputs B0, B1 and B2 are routed through data selector U28. With a high from range zero decoder U27-3, these levels are applied directly to Control Logic U12. With U27-3 low, U28 ignores these levels and applies a low to M1 and M2 and a high to M3 in Control Logic. Output B3 is low only during CPM operation, when it is used to disable RESOLUTION settings, blank decimal points and units annunciators, and route 1/6 MHz to Control Logic. Output B4 is low only when FREQ C is selected (refer to Time Interval Average Logic for an explanation). Provided the lowest RESOLUTION (10^0) is not selected output B6 enables program inverter U6-8 during ratio and period averaging measurements. The final output from U38, B7, enables the output from gate synchronizer U4-6 during FREQ A and CPM modes.

Table 3-3. Function Decoding (U38)

	INPUTS						OUTPUTS							
	A_4	A_3	A_2	A_1	A_0	ENABLE	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
FREQ A	0	0	0	0	0	0	1	0	1	1	1	0	0	0
RATIO A/B	0	0	0	0	1	0	0	0	1	1	1	0	0	1
PER A	0	0	0	1	0	0	0	0	1	1	1	0	1	0
PER AVG A	0	0	0	1	1	0	0	0	1	1	1	0	1	1
TI	0	0	1	0	0	0	1	0	1	1	1	1	0	0
TIA	0	0	1	0	1	0	1	0	0	1	1	0	1	1
FREQ C	0	0	1	1	0	0	1	0	1	0	1	0	0	0
CHK	0	0	1	1	1	0	0	0	1	1	1	1	1	1
CPM	0	1	0	0	0	0	1	0	1	1	0	0	0	0
TOT A·B	0	1	1	1	0	0	0	0	1	1	1	1	1	0
FREQ A	1	0	0	0	0	0	1	0	1	1	1	0	0	0
RATIO A/B	1	0	0	0	1	0	0	1	1	1	1	0	0	1
PER A	1	0	0	1	0	0	0	0	1	1	1	0	1	0
PER AVG A	1	0	0	1	1	0	0	1	1	1	1	0	1	1
TI	1	0	1	0	0	0	1	0	1	1	1	1	0	0
TIA	1	0	1	0	1	0	1	0	0	1	1	0	1	1
FREQ C	1	0	1	1	0	0	1	0	1	0	1	0	0	0
CHK	1	0	1	1	1	0	0	0	1	1	1	1	1	1
CPM	1	1	0	0	0	0	1	0	1	1	0	0	0	0
TOT A·B	1	1	1	1	0	0	0	0	1	1	1	1	1	0
		F8	F4	F2	F1									

3-45. Time Interval Logic

3-46. In the Time Interval function, the Main Gate flip-flop U3-9 is held high, and Main Gate enabling is controlled entirely by two D flip-flops (U36-6 for interval start, U36-9 for interval stop). Figure 3-12 illustrates time interval circuitry. Main Gate clocking is provided by the instrument's time base; clocking frequencies from 10 MHz through 100 Hz (respective settings of 100 ns through 10 ms) are selectable with the RESOLUTION control. Control Logic pin EH goes high when 100 ns is selected; the 10 MHz reference is thus fed to the Main Gate. In all other RESOLUTION settings for Time Interval mode, EH is low, and Main Gate clocking is provided from the divided time base at Control Logic pin CO.

3-47. In the initial state, start flip-flop U36-6 can be clocked by the Channel A signal provided Time Interval has been selected, Main Gate GQ is low, and U18-9 is low. Once clocked, U36-6 goes low to enable the Main Gate. A stop pulse on Channel B must now be applied to clock U36-9 high, ending the Main Gate enable. With Control Logic pin TE high in Time Interval mode, the stop flip-flop D input is high whenever start flip-flop U36-5 is clocked high by the Channel A signal. If not held clear by time interval holdoff gate U16-3, stop flip-flop U36-9 will now go high with the next available pulse on Channel B and the Main Gate will be disabled. Control Logic will respond by waiting 0.1 ms and providing a memory update command ($\overline{M}$).

3-48. Time Interval Average Logic

3-49. During time interval average measurements, the 7260A counts the 10 MHz reference frequency (all RESOLUTION settings) and the number of intervals to be averaged. The total count of the 10 MHz reference is displayed when the number of intervals (10^0-10^5) selected by the RESOLUTION control has been satisfied. Relevant circuitry is illustrated in Figure 3-12. Generally, the Main Gate is controlled by the Time Interval Flip-Flops in the same manner as with Time Interval measurements. Control Logic functions in essentially the same fashion as with Period Average measurement. In Time Interval Average, Control Logic maintains a 200 nsec "dead time" between measurement cycles.

3-50. With Control Logic set for Period Average type measurements, pins EH and CO are held high. The 10 MHz reference is thereby routed through U20-3 and U10-11 to clock the Main Gate (U7).

3-51. Enabling of the Main Gate for clocked operation is controlled by the Time Interval Flip-Flops. With U36-6 and U36-9 low, clocked operation is enabled. With either flip-flop output high, the Main Gate is disabled. The start flip-flop, U36-6, can be clocked by the Channel A signal when the following conditions are met: TI or TIA is selected, GQ from the Main Gate Flip-Flop U23-7 is low, and U18-9 is low. With these conditions met, U36-6 goes low and, provided U36-9 is also low, the Main Gate (U7) will begin counting the 10 MHz reference.

3-52. The stop flip-flop (U36-9) can be clocked by the Channel B signal (XB) only when a number of inputs are satisfied. To release the clear input, U35-12 must go high. This condition is met only when the three inputs to U35-12 are high. The first input, from U21-9, is high when TI or TIA is selected and U18-9 is high.

3-53. The second input, U25-12, provides start before stop logic. If a start pulse has not been received, U26-4 will be high. A high will also be present from U10-6 when the term TI + (TIA·R0) is false. In this instance, a stop pulse applies a high from U26-2, U25-12 goes low, and the stop flip-flop is held clear. Once a start pulse is received, U26-4 is low and U25-12 is held high; the stop flip-flop is no longer held clear.

3-54. The third input to U35-12 involves the 7260A's time interval holdoff feature, which serves to hold the stop flip-flop clear for a period of time after the start flip-flop has been clocked. The Holdoff Enable line goes true when the front panel HOLDOFF control is on. To satisfy the needed high condition to U35-12, either the HOLDOFF control must be off, or, if it is on, U3-5 must be high. Timer U23-9 operation is initiated by a start pulse clocking U36-5 high. The timer will clock holdoff flip-flop U3-5 high after a duration set by the front panel control. When enabled, TI HOLDOFF keeps the stop flip-flop cleared for a period ranging from 20 μs (fully ccw) to 20 ms or greater (fully cw).

3-55. When TIA operation is first selected, Main Gate flip-flop (U23) output GQ is initially high; the following circuit conditions exist:

1. NAND gate U20-12 is enabled, allowing a 100 kHz signal to feed monostable multivibrator U34-2.

2. Start flip-flop U36-6 is held cleared. The start Q output to the Main Gate (U7) is thus high and no counting of the 10 MHz clock is possible.

3. Holdoff flip-flop U3-5 is cleared.

4. Stop flip-flop U36-9 is cleared through U21-8. The stop Q output to the Main Gate is low.

5. Gate light drive circuits are enabled at U21-5.

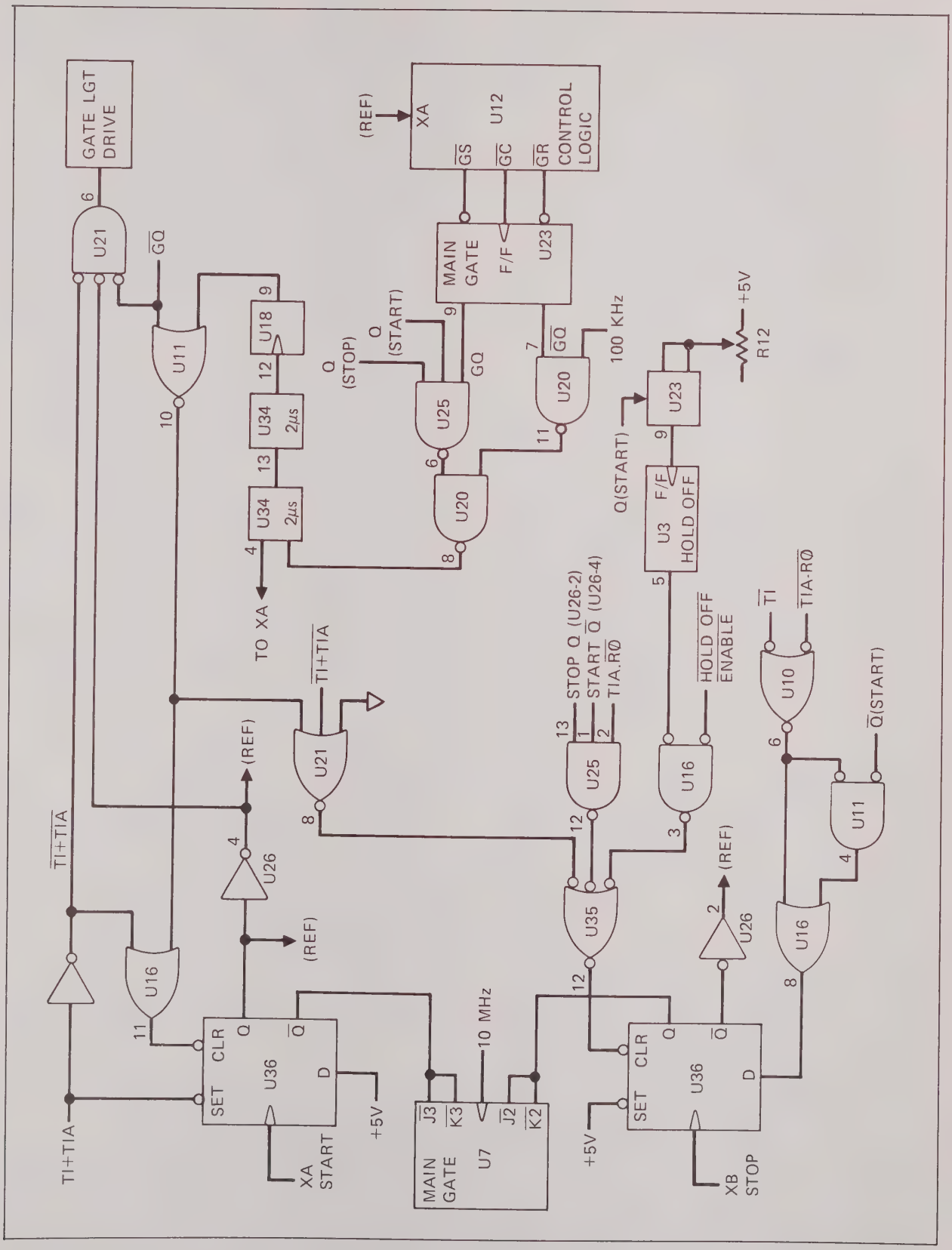


Figure 3-12. Time Interval Average Logic

3-56. The 100 kHz signal is briefly fed to Control Logic (U12) input XA. The resultant first clocking of the Main Gate Flip-Flop shifts GQ low, causing the following circuit conditions:

1. NAND gate U20-11 is disabled and the 100 kHz is no longer supplied to Control Logic.

2. The clear input to start flip-flop U36-6 goes high. A start pulse from Channel A will now be able to clock U36-3.

3. The clear input to time interval holdoff flip-flop U3-5 goes high. When applied, a holdoff setting can now keep stop flip-flop U36-9 cleared.

4. The clear input to stop flip-flop U36-9 goes high. With other conditions met, a stop pulse on Channel B will now be able to clock U36-11.

3-57. Monostable multivibrator U34-13 sends a 2 μsec count pulse to the XA input of Control Logic for each interval measured. At the end of each time interval measurement, U18-9 goes high to clear the time interval start flip-flop. The count is increased by one in the Control Logic interval counter. This sub-cycle will continue until the count in the interval counter reaches the number of time intervals selected for averaging by positioning of the front panel RESOLUTION control (10^0-10^5). At that time, Control Logic clocks the Main Gate flip-flop, GQ goes low and the measurement cycle ends. Counter multiplexer U13 holds the total count accumulated during all the time intervals measured until Control Logic (U13) outputs a memory update ($\overline{M}$) signal. The RESOLUTION control position determines the decimal point position and the number of intervals involved in the measurement cycle. Automatic averaging of the total count results from this positioning. Control Logic waits through the 250 msec recycle time and begins another measurement cycle.

3-58. Frequency C Logic (520 MHz Direct)

3-59. Refer to Figure 3-13 during the following circuit discussion. During Frequency C measurements, the 7260A will use an output from the Channel C option as an input for a Frequency A measurement. To accomplish this, function decoding must both set Control Logic (U12) for Frequency A and provide separate logic control for the adjusted signal path. Decoder ROM U38 satisfies these two requirements. First, function lines F1, F2, F4 and F8 are decoded to encode Control Logic (U12) inputs M1, M2 and M3 for Frequency A measurements. Secondly, U38 output B4 supplies control signal $\overline{FC}$. The $\overline{FC}$ output first disables Channel A and B Signal Conditioners. With C Direct true whenever the 520 MHz Option is installed, U11-1 and U11-13 clear gate synchronizer U4-6. Since Control Logic output EA is high in Frequency A, $\overline{FC}$ must also be used to disable any Channel A input from reaching the 7260A's Main Gate (through U10-8). Output $\overline{FC}$ true also enables the digit 1 carry signal from the Channel C Option. The Channel C input is first decade divided on the option pcb. The carry 1 output from this first BCD coded digit (CECL) is applied through U14-3 to the 7260A's digit 1 count circuits. These circuits now become digit 2 count circuits. BCD outputs from digit 1 and 2 in Frequency C are routed through the Option PCB and applied to 7260A counter multiplexer U13.

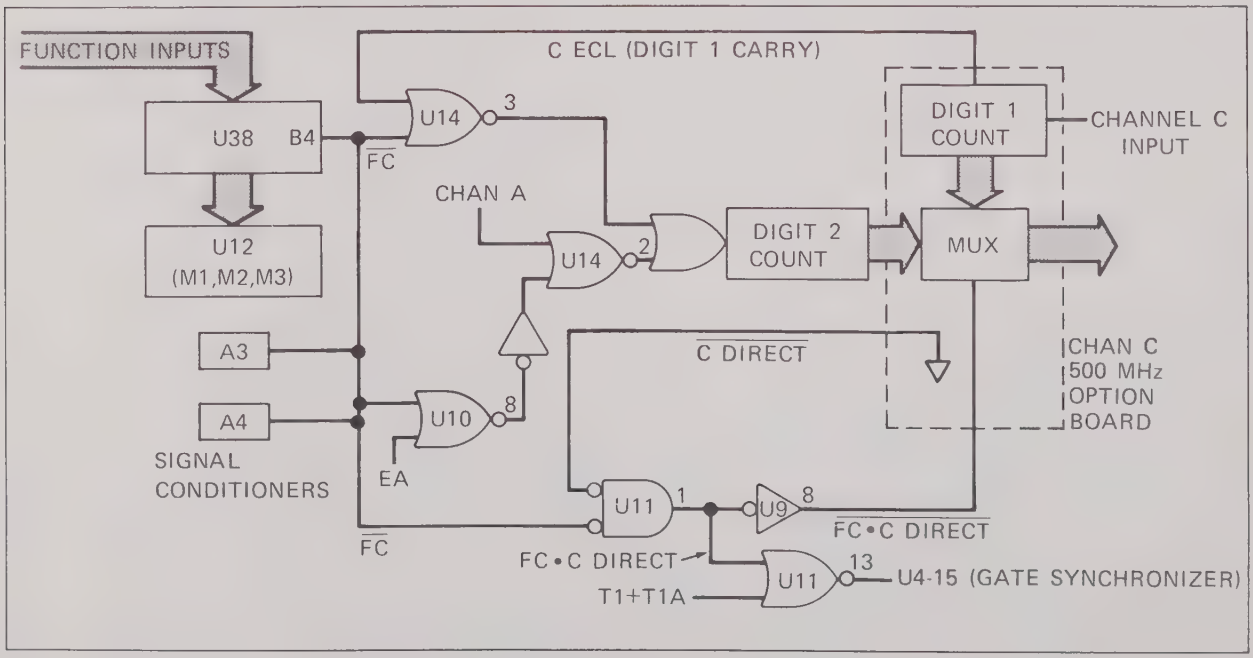


Figure 3-13. Frequency C Logic

3-60. Resolution Logic

3-61. Resolution settings can be established from either the front panel or through the Data I/O Unit (Option - 521). In either case, logic levels are set for lines R1, R2 and R4. These levels, routed through multiplexer U29, are decoded within Control Logic to enable one of six decade dividers. A choice of gate times is thereby provided. Each change of the front panel RESOLUTION switch also generates a range reset using the reset multivibrator U24-12. The three selected resolution levels, normally routed directly through U29, are disabled in Counts per Minute mode. With this mode selected, the CPM signal decoded by U38 goes false, and U29 outputs become dependent on preset levels. Table 3-4 defines U29 multiplexer inputs and outputs.

Table 3-4. Multiplier Inputs/Outputs (U28, U29)

STR	SEL	A (1A, 2A, 3A)	B (1B, 2B, 3B)	Y (1Y, 2Y, 3Y)
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

A = Preset Input
B = Variable Input
Y = Output to Control Logic

3-62. During autoranging, Control Logic will sequence once through the available resolution settings. The sequence will stop when the Most Significant Digit (MSD) is filled or when the maximum gate time allowed has been reached. Autoranging can be enabled only during FREQ A, RATIO, PER, PER AVG A, TI or CHK operations. Measurement unit annunciators and decimal points will not be changed during autoranging. An iteration counter within Control Logic will step through the possible resolution settings. A measurement sequence is initiated for each step; if, at the end of a sequence, the counter is not set to the last resolution step, either a new measurement sequence is begun at the next higher resolution or the display is updated (if not in overflow).

3-63. When the reading is only marginally best resolved in one setting, or is varying slightly, an unnecessary shift in resolution will be prevented by a hysteresis circuit in Control Logic U12. The hysteresis flip-flop becomes activated when the MSD reaches 1; the resolution will be held until the Second Significant Digit (2SD) falls below 8. The circuit thereby allows input frequency changes of up to 20% to occur without resolution change.

3-64. Resolution Logic - 10^0 Setting

3-65. Unique function dependent operations take place when the RESOLUTION control is set to 10^0. Refer to Figure 3-14 during the following circuit description:

1. The first output, termed R0 at U27-8, is used as the A4 input to decoding ROM U38. With resolution 10^0 selected, R0 will be low. If Time Interval Average is also selected, U38 will output a low to U27-2. Function multiplexer U28 is thereby set to its predefined state by U27-3 going low; Control Logic is set to the Time Interval mode.

2. Secondly, if U38 decodes R0 at A4 and either Ratio or Period Average is selected on A0-A3, ROM decoder output B6 places a high at U6-9. The gate U6-8 thereby acts as a program inverter to allow count stabilization within Control Logic.

3-66. Control Logic

3-67. The Control Logic integrated circuit (U12) provides most of the logic and timing requirements for the 7260A. When used in conjunction with decoding ROM U38 and function data selector U28, U12 determines most function related operations. With resolution selector U29, U12 determines main gate frequency and decimal point placement. In the following paragraphs, general Control Logic operations inputs and outputs will be discussed. A brief description of pin designations is presented in Table 3-5.

3-68. Control Logic provides six decade counters. Inputs and outputs for the counters are defined by function in Table 3-6. Outputs at pin GC will, by clocking the Main Gate Flip-Flop, enable the Main Gate. Outputs at pin CO will clock the Main Gate. Control Logic will also provide certain gating control signals. Refer to "Main Gate Logic" and "Main Gate Enabling Logic" for descriptions.

3-69. A general reset ($\overline{R}$) is sourced by Control Logic whenever a measurement cycle is complete or a function change is decoded. A reset input to Control Logic at RI will have the same affect. Such inputs may be provided by the front panel RESET control, an optional remote interface, the range reset monostable multivibrator U24-12, the power-on reset multivibrator U24-4 or a Channel C option assembly. An $\overline{R}$ signal will reset the eight display decade counters, along with the overflow flip-flop in Counter Multiplexer U13. The display is consequently set to zero and a new measurement cycle is initiated. The remote start signal (ST) differs from the RI input in that a new measurement sequence is begun without the display being set to zero.

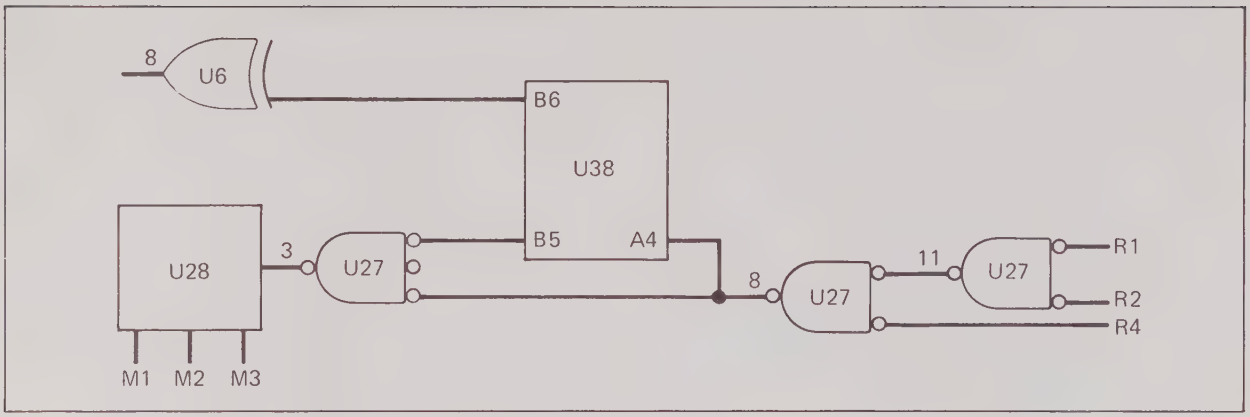


Figure 3-14. Resolution 10^0 Logic

Table 3-4. Control Pin Designations

PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
1	Vss	+5V, +/–0.25V	25	EH	Output, enables 10 MHz clock for CHK (all resolutions) and TI A-B or PER (100 ns resolution only)
2	D1	Input, Strobe Line DS2			
3	D2	Input, DS3			
4	D3	Input, DS4			
5	DP	Output, decimal point multiplexed to strobe lines	26	$\overline{GR}$	Output, resets Main Gate Flip-Flop and set Time Interval start flip-flop
6	UX	Output, units annunciator multiplexed from FUNCTION and RESOLUTION settings	27	$\overline{GS}$	Output, sets Main Gate Flip-Flop, stays high in CHK and TOT A-B
7	RI	Input, reset			
8	D4	Input, DS5	28	CO	Output, from decades in PER or TI A-B
9	D5	Input, DS6			
10	D6	Input, DS7	29	Vgg	0V
11	Vdd	–12V, +/–1V	30	ST	Input, start from remote
12	CI	Input, 1 MHz (1// MHz in CPM mode	31	SC	Input, single or continuous counts from remote
13	P2	Prescaler control	32	$\overline{M}$	Output, memory update to Counter-Multiplexer U15
14	P1	bits (used with FREQ C)			
15	XB	Input, from Channel B Signal Conditioner. Used in RATIO A/B	33	BY	Output, Busy (high) when a measurement sequence in process
			34	CR	Cycle Rate RC setting
16	XA	Input, from Channel A Signal Conditioner. Used in PER, PER AVG A.	35	$\overline{R}$	Output, resets decade counter
			36	AR	Input, autorange feedback from Counter- Multiplexer U15
17	EA	Output, LO for TI A-B and CHK	37	TQ	Input, from time interval stop flip-flop at end of measurement
18	TE	Output, HI for TI A-B	38	GQ	Input, from output of Main Gate Flip-Flop
19	M1	Inputs, FUNCTION lines from front panel control			
20	M2		39	AO	Input, autorange feedback from overflow flip-flop in Counter-Multiplexer U15
21	M3				
22	R1	Inputs, RESOLUTION lines from front panel control			
23	R2		40	GC	Output, clocks Main Gate Flip-Flop at frequency from 1 MHz through 10 Hz when in TI A-B or PER mode
24	R3				

Table 3-6. Control Logic Decade Inputs, Outputs

FUNCTION	INPUT DESCRIPTION	OUTPUT DESCRIPTION
FREQ A	10 kHz derived from input of 1 MHz at CI	10 kHz to 0.1 Hz in 6 decade steps at GC
CPM	1/6 MHz at CI	1 2/3 Hz at GC
RATIO A/B	Channel B input (5 Hz ⟶ 1 MHz)	1 of 6 decades at GC
PER A	1 MHz at CI	1 MHz to 10 Hz in 6 decade steps at GC
PER AVG A	Channel A input (5 Hz ⟶ 1 MHz)	1 of 6 decades at CO
TI A-B	1 MHz at CI	1 MHz to 10 Hz in 6 decade steps at CO
TIA A-B	Pulse from U34-4 for each interval	When number of intervals counted matches number selected, GC clocks Main Gate F/F.
TOT A-B	Not used	High at GC
CHK	10 kHz derived from input of 1 MHz at CI	10 kHz to 0.1 Hz in 6 decade steps at GC

3-70. The decimal point (dp) output is controlled by both the decoded RESOLUTION setting and the strobe inputs from counter-multiplexer U13. The measurement cycle rate (time between successive measurements) is determined by an exterior RC network connected to pin CR. The 7260A will normally start a new measurement cycle automatically. An input high on pin SC will allow Control Logic to stop after one measurement (single reading mode). This feature is controlled by a remote start/stop command.

3-71. When set for autoranging, Control Logic utilizes two feedback paths to the Counter-Multiplexer U13 AO-AR. An internal iteration counter will step through the available resolutions until a Carry 6 is seen on AR or until the lowest resolution step has been reached. Autoranging is not available in TOT A or CPM X100A. An internal hysteresis flip-flop; is connected to line AO to prevent needless resolution changes during marginal or slightly varying inputs. An internal 14 stage static shift register controls sequencing during the measurement cycle.

3-72. Main Gate Clocking Logic

3-73. The clocking input to the Main gate is supplied by one of four sources, as specifically defined in Table 3-1. Figure 3-15 provides a simplified schematic diagram of clocking circuits. With Control Logic (U12) output EA high, the Channel A input is used as the clocking source during FREQ A, CPM, RATIO A/B and TOT A•B measurements. Output EA is held low to inhibit the Channel A signal during period (PER A or PER AVG A), time interval (TI or TIA), or self check measurements. Except during the highest resolution, PER A, TI measurements receive clock inputs from the decade divided time base (output CO from Control Logic U12). During the highest resolution, EH is held high, and the 10 MHz time base is used directly. During TIA, PER AVG A and CHK, EH is held high continuously to feed the 10 MHz time base to the Main Gate. With Control Logic set for a Frequency A type measurement during FREQ C, EA will be high. Decoder ROM (U38) output $\overline{FC}$ is therefore used to disable the Channel A input. A signal from the optional Channel C pcb is then routed to the Main Gate clock.

3-74. Main Gate Enabling Logic

3-75. Figure 3-16 provides a simplified schematic version of gate select circuitry. The Main Gate (U7) is a multiple J, K and clock input flip-flop. It will be enabled for clocked operation when all J and K inputs are low. Any one set of J and K input going high will disable clocked operation. In modes other than TI and TIA, inputs to J2, K2, J3 and K3 are always low; gate selector U47-8 controls Main Gate Enabling. The gate enabling inputs are summarized in Table 3-1. During FREQ A, FREQ C, CPM, TI or TIA modes, the B7 output from decoder U38 is high; gate synchronizer U4-6 synchronizes the main gate flip-flop outputs (GQ and $\overline{GQ}$) to the time base derived 100 kHz. The B7 output goes low in RATIO, PER, PER AVG A, TOT and CHK. Gate synchronizer outputs are now disabled, and the GQ gate enable signal is fed directly to J1 and K1 in the Main Gate.

3-76. Count Circuits

3-77. The Main Gate clocking signal is serially applied to eight BCD counters. Bit 1 information for Digit 1 is provided by the Main Gate flip-flop (divide-by-two). This data is converted to TTL levels by Q1 and Q2 and applied to three J-K flip-flops (U5-91 for Bit 2, U5-51 for Bit 4, U4-9 for Bit 8). These four bits are applied to a tri-state buffer (U22) and to the Channel C option (if installed).

The fourth bit is also applied to BCD counter U32 for derivation of Digit 2 information. The four bits for Digit 2 provide the remaining inputs to the tri-state buffer. In most functions, the Digit 1 and Digit 2 information will be passed through U22 and applied to Counter-Latch-Multiplexer U13. If the instrument is in Frequency C mode and the 520 MHz Direct, Option -310, is installed, U22 will be disabled; Digit 1 and 2 information will then be provided by the Option.

3-78. The remaining six digits (D3-D8) are derived within Counter-Latch-Multiplexer U13. Figure 3-17 provides a simplified schematic diagram of U13. Digit 1 and Digit 2 are applied to separate 4-bit latches. Digit 2 carry is also applied to the Digit 3 BCD counter. Digits 4-8 are derived from similar counters and applied to 4-bit latches upon receipt of the Memory Update ($\overline{M}$) signal from Control Logic (U13). Any overflow condition (defined as a Carry 8) will be applied to the 1 bit overflow latch at the same time.

3-79. A scan counter within U15 controls latched digit outputs and strobes. This counter is driven by an internal oscillator whose frequency is determined by the external connection of C16. As the 4-bit contents of each latch (Digit 1-8) is scanned for output, a simultaneous strobe signal (DS1 -DS8) is applied to the appropriate display digit. The contents of all eight latches are thus sequentially displayed. Decimal point placement is provided exterior to U13 by Control Logic (U12).

3-80. Display

3-81. The output from Counter-Multiplexer, U15, is applied, through BCD-to-Seven Segment Decoder U35, to all display digits. A strobed output from U15 on lines DS1-DS8 enables the appropriate digit through drivers U40 and U41. In overflow conditions, a latched output is applied directly to the OVFL LED. Control Logic (U12) monitors strobe lines DS1-DS8 to provide decimal point (DP) placement following the correct display digit. Measurement unit (UX) display inputs are supplied by Control Logic function and resolution decoding circuits.

3-82. Reference Inputs and Outputs

3-83. The 7260A's rear panel provides four BNC connections: MARKER OUT, 10 MHz REF IN and OUT and TRIGGER LEVEL OUT. The MARKER OUT connector provides a high true representation (100 mV into 50 ohms) of the time between a start pulse on Channel A and a stop pulse on Channel B for use in Time Interval measurements. Specifically, marker output generator U42-5 is clocked high by a slope selected pulse on Channel A, clearing U42-13. A slope selected pulse on Channel B will have the opposite effect by clearing U42-1 and bringing U42-5 low.

3-84. The 10 MHz REF IN connector receives an external signal for use as the 7260A's time base when the INT/EXT switch is set to EXT. Inputs ranging from 300 mV to 3.0V rms are shaped by Schmitt trigger U37-2 to provide a pulsed reference for the instrument's internal circuitry.

3-85. The 10 MHz REF OUT connector provides a shaped output of the instrument's time base frequency, internal or external. Output buffer U37-10 supplies a nominal signal level of .5V or greater into 50 ohms.

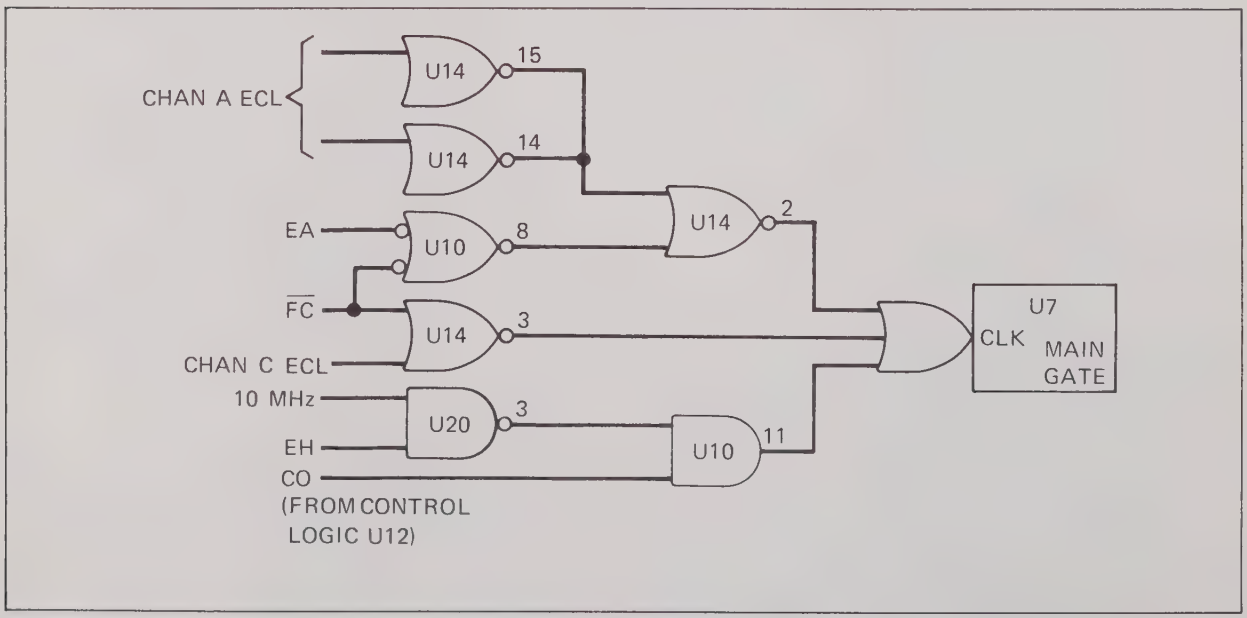


Figure 3-15. Clock Select Logic

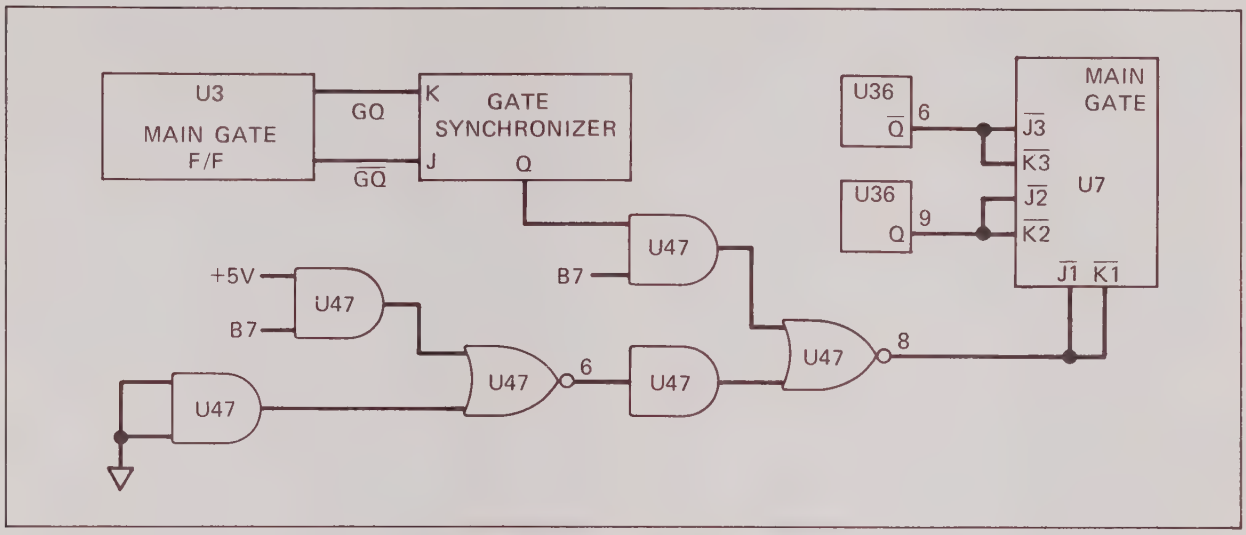


Figure 3-16. Gate Select Logic

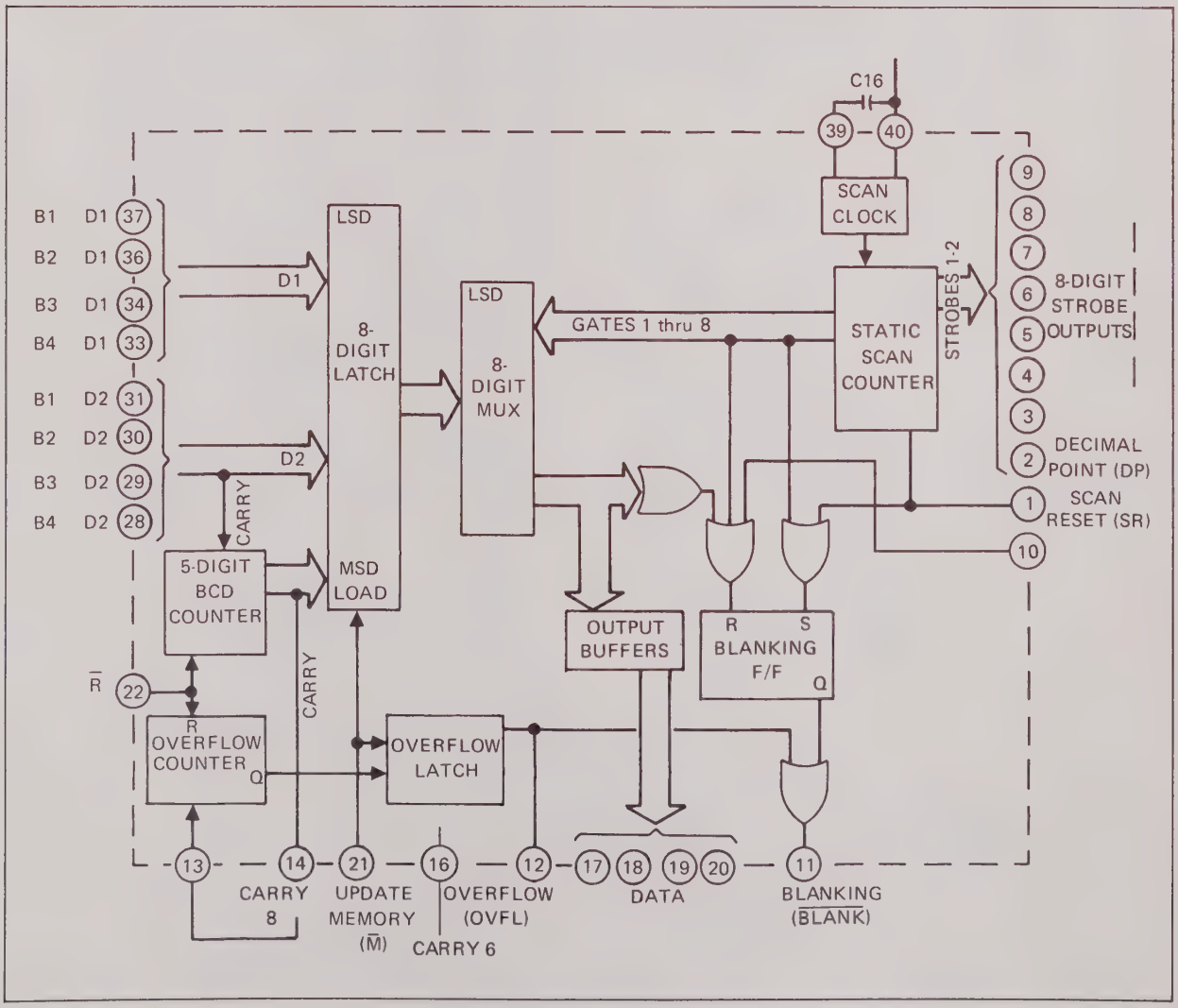


Figure 3-17. Counter Multiplexer (U13)

3-86. The instrument's TRIGGER LEVEL OUT connector provides a switch selected sampling of the Channel A or Channel B trigger level, as determined by the front panel TRIGGER LEVEL controls.

3-87. Reset Logic

3-88. Reset from Control Logic ($\overline{R}$) clears the decade counters and initializes the display latches. The reset input (RI) to Control Logic is derived in one of four ways. The front panel RESET switch controls RI for as long as it is held depressed. A power on reset will be provided to RI to allow for stabilization of the 7260A's power supply voltages. Monostable multivibrator U24-4 provides time delay and pulse shaping for this reset. A change in the front panel RESOLUTION setting will cause a reset from the multivibrator U24-12. A remote reset will cause the same reset operations as does the RESET switch. Internally, Control Logic (U12) will generate its own $\overline{R}$ whenever a FUNCTION change is decoded. Use of the RESET switch or a remote reset will also place display decoder U31 in lamp test mode; all eight display digits will read "8" for as long as this reset is held applied.

3-89. Gate Indicator Logic

3-90. The gate light circuit, as illustrated in Figure 3-18, provides a visual indication of the Main Gate being enabled. Data selector U33 provides gate signal source decoding to timer U23. If Time Interval or Time Interval Average is selected, output W from U33 will be low to trigger U23 whenever input D2 is high. This high is provided by D flip-flop U18-6 when Main Gate Flip-Flop GQ is low, TI or TIA has been selected and the start flip-flop Q goes low. A gate indication is thereby provided with each interval start pulse. If TOT A•B mode is selected, output W is low (due to a constant D7 input high from Control Logic pin EA), and the GATE light is illuminated when Channel B input requirements are satisfied. In all functions, output W is low whenever GQ from the Main Gate flip-flop is high. Timer U23 provides a gate light stretching function by providing a minimum 50 μsec gate pulse (G); visual discernibility is thereby ensured.

3-91. Single/Continuous Operation

3-92. The instrument can be programmed to either initiate measurement cycles continuously at a predetermined rate (continuous operation) or initiate one and only one measurement cycle when signaled by the start circuit on the Main PCB (this start circuit is not the same as the START Gate used by the Time Interval circuit). When the instrument is under local control, single or continuous operation is selected by the Rear Panel MODE switch. Remote Operation is described later in this section. When the MODE switch is in the CONT position, the SC (single/continuous) and ST (start) signals from U43 to Control Logic are both low. This commands Control Logic to continuously initiate measurement cycles at a predetermined rate. If the MODE switch is in the TRIG position, SC is high, commanding Control Logic to wait for a high level on the ST line before initiating a measurement cycle. With the MODE switch in the TRIG position, ST is determined by U17-6. If any function except FREQ C is selected, U17-6 is controlled by XB. When there is a signal on Channel B, Control Logic will be commanded to initiate a measurement cycle. If the Channel C function is selected, U17-6 will be high if the amplitude of the signal applied to the Channel C input is above the threshold level. As long as the amplitude of the Channel C input signal remains above the threshold level, Control Logic will operate as if the continuous operation function has been selected. If the amplitude of the Channel C input signal drops below the threshold level, U17-6 is low, ST is low and Control Logic is prevented from initiating another measurement cycle.

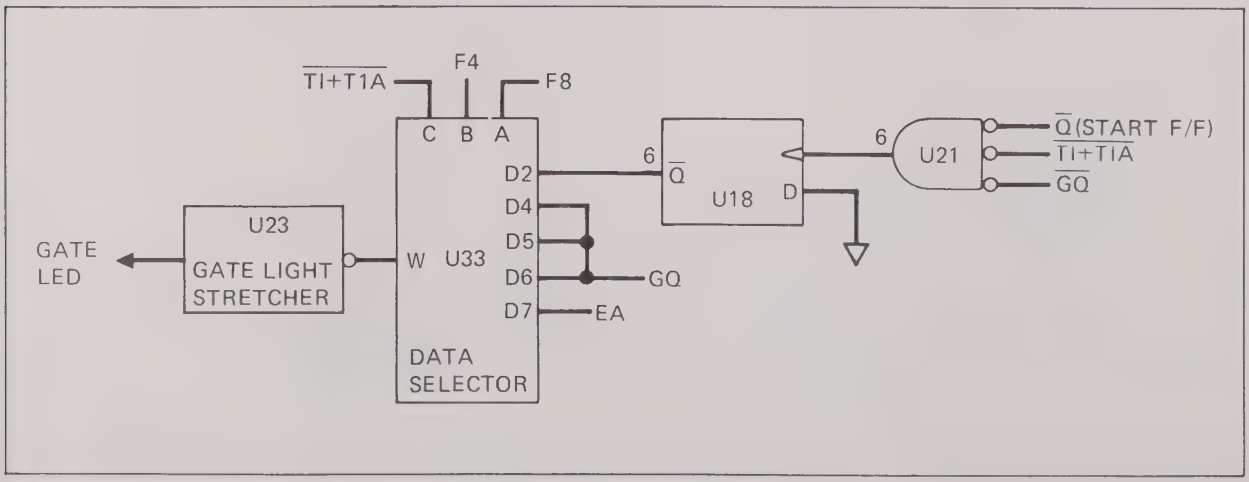


Figure 3-18. Gate Indicator Circuits

3-93. Remote Logic

3-94. Bidirectional data may be exchanged through the Data I/O Unit (Option -521). The 7260A outputs strobe, annunciators and BCD digit information, and receives programming inputs - function, resolution, slope, filter and reading mode commands (STR, SCR). All connections are present at P4 on the Main PCB. Refer to Figure 3-19 for a simplified view of remote logic. Remote operation is selected when the remote interface sets the $\overline{\text{REM}}$ line true. Three effects of this action are felt. The inverted $\overline{\text{REM}}$ signal first sets tri-state buffers U39 and U30 for open-collector operation. Locally sourced resolution, function, slope and filter commands are thereby ignored, and their remote counterparts directly control 7260A operation. Secondly, the inverted $\overline{\text{REM}}$ signal disables the front panel RESET control. Finally, data selector U43 is set to provide ST and SC inputs to Control Logic. If the rear panel reading mode control is set to CONT, the ST output reflects the STR input and the SC output follows the SCR input. With TRIG selected, the SC output remains high, and the ST output becomes dependent on the state of U17-6.

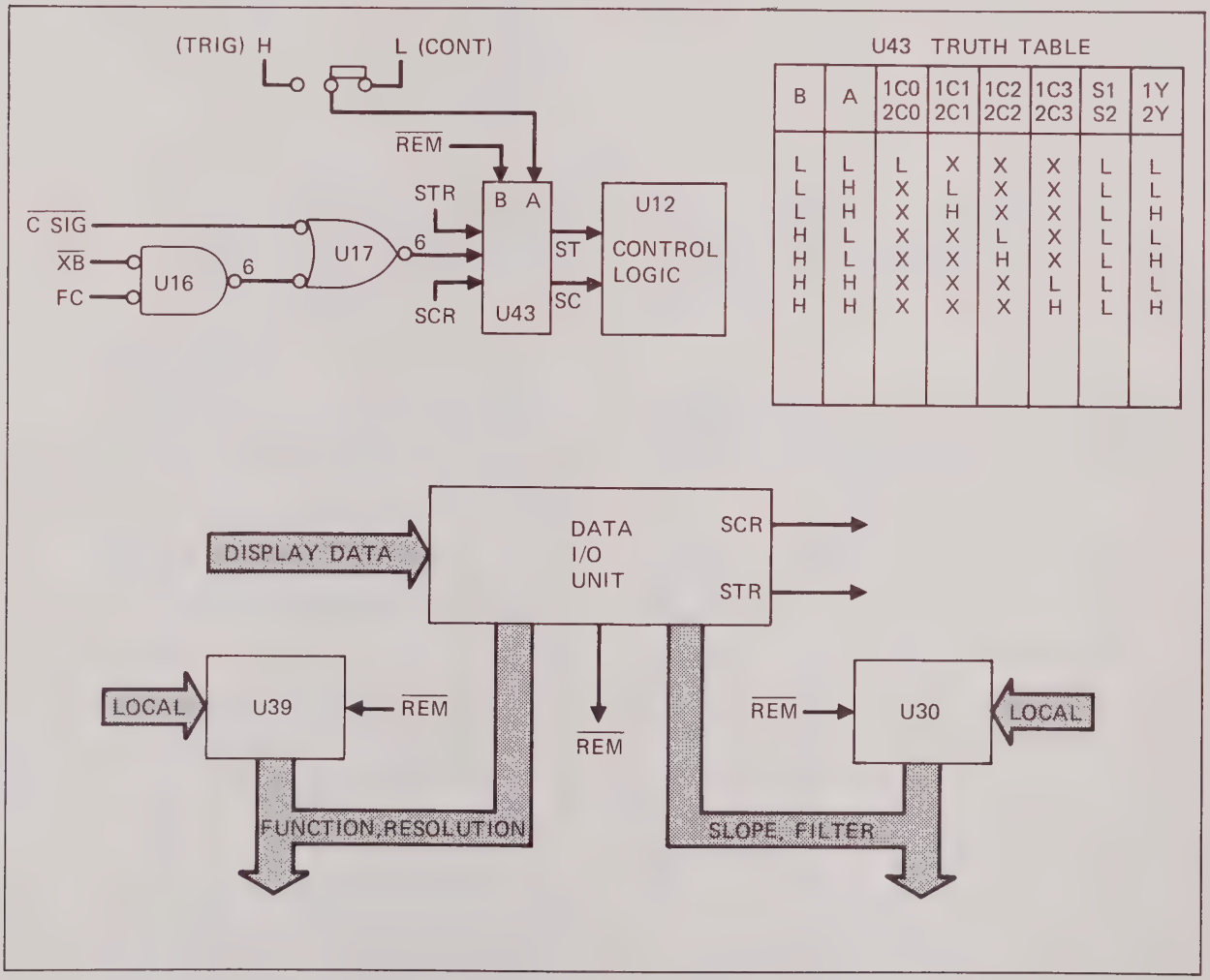


Figure 3-19. Remote Logic

Section 4
Maintenance

WARNING

THESE SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID ELECTRIC SHOCK, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN THE OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

4-1. INTRODUCTION

4-2. This section of the manual provides information concerning warranty, general maintenance, performance tests, calibration and troubleshooting for the 7260A Universal Counter/Timer. Test equipment recommended for performance tests, calibration, and troubleshooting is listed in Table 4-1. If the recommended equipment is not available, equipment with equivalent specifications may be used. Test points and adjustments on the Main PCB are illustrated at the end of this section.

4-3. SERVICE INFORMATION

4-4. The instrument is warranted for a period of one year upon delivery to the original purchaser. The WARRANTY is located on the back of the title page of this manual.

4-5. Factory authorized calibration and service for each Fluke product is available at various worldwide locations. A complete list of these service centers is included in Section 7 of this manual. If requested, an estimate will be provided to the customer before any work is begun on instruments that are beyond the warranty period.

4-6. GENERAL MAINTENANCE

NOTE

To avoid contaminating the pcbs with oil from the fingers, handle the pcbs by their edges or wear gloves. If a pcb does become contaminated, refer to the cleaning procedure.

Table 4-1. Required Test Equipment

EQUIPMENT TYPE	REQUIRED SPECIFICATIONS	RECOMMENDED TYPE
Oscilloscope	Dual trace, DC-200 MHz wideband	Tektronix 475
High Frequency Signal Generator	10 MHz-125 MHz <10 mV rms	Wavetek 2001
Low Frequency Signal Generator	Up to 10 MHz at a level of 1V rms. Time base 1 x 10^{-8} per day.	Fluke 6011A
50Ω Terminator (3)	Impedance match the UUT.	GR874
Digital Multimeter	AC volts up to 250V ac. DC volts to 1V ±0.01V rms. Resistance - 0 to infinity.	Fluke 8012A
50Ω Adapter	Impedance match UUT to RF Voltmeter.	Boonton 91-8B
Oscilloscope Probe	X10	Tektronix P6065A
3-way Splitter	50Ω	HP11667A
RF Voltmeter	125 MHz, 10 mV rms to 5V rms.	Boonton 92BD

4-7. Disassembly

4-8. To disassemble the instrument, use the following procedure:

1. Press the power switch to STBY, and remove the line power cord.

2. On the case bottom, remove the six securing screws. Two of these screws will be found in the middle of the case, under the latches. To access either middle screw, as shown in Figure 4-1, alternately push the two latching rails away from the triangular stop. Pull the latch out far enough to reveal the screws.

3. The top half of the case may now be separated from the bottom.

NOTE

Do not hold the case bottom while lifting off the case top. Damage to the Main PCB could otherwise result.

Alternating between front and rear panels, pry the case top free of the rest of the instrument. In the front, press down on the BNC input connectors, while gently pulling up on the case top lip. In the rear, press down on the heatsink, while pulling up on the top case lip.

NOTE

For most test and calibration procedures, stop at this step.

4. Remove the single screw at the middle of the Main PCB, and separate the case bottom.

5. Remove the Signal Conditioner Assemblies (A3 and A4) from connectors on the Main PCB and the Front Panel PCB. Pry either assembly gently away from its Front Panel Connector until free. With a gentle rocking motion, now lift the assembly out of its Main PCB connector. Avoid bending individual connector pins on the Signal Conditioners.

NOTE

The Signal Conditioners must not be interchanged. Each assembly is component matched to a hysteresis resistor on the Main PCB.

6. To remove the Front Panel Assembly from the Main PCB Assembly, first pull off the following switch buttons in the panel's lower left corner:

a. ON - STBY (green)

b. BAT - LINE (white)

c. RESET (blue)

7. Gently pry the Front Panel Assembly away from its 40-pin connector (left) and guide pin (right). Avoid bending individual connector pins on the Main PCB.

8. Refer to Section 6 of this manual when removing any optional assemblies.

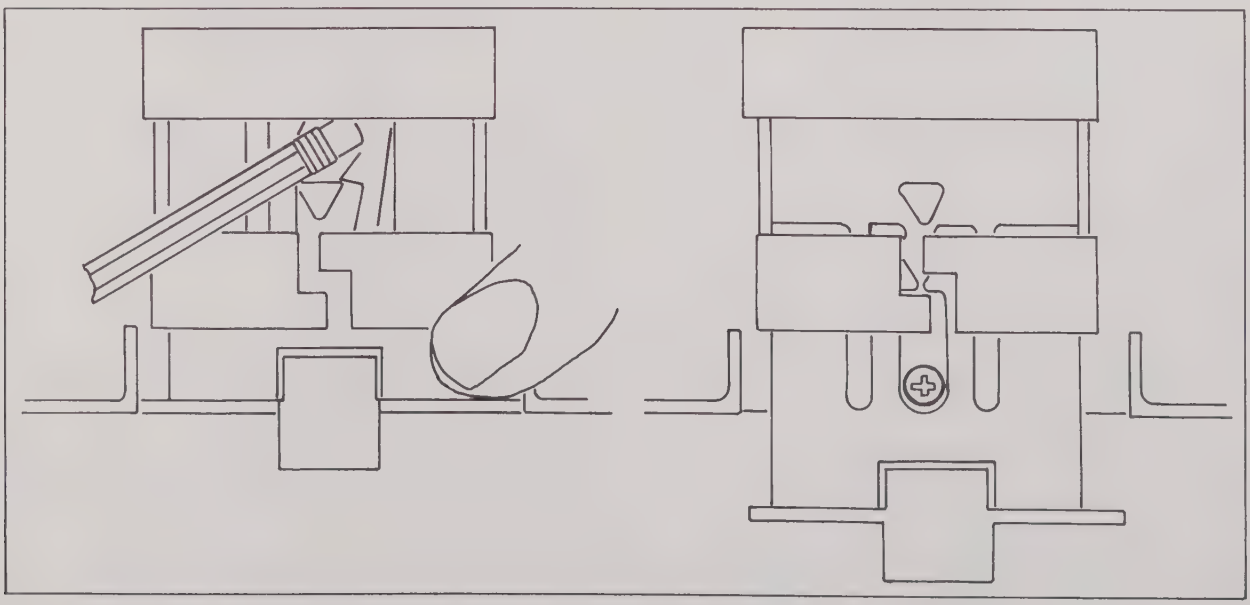


Figure 4-1. Latch Removal

4-9. Reassembly

4-10. For reassembly, the disassembly procedures can generally be followed in reverse. Keep the following considerations in mind:

1. When reinstalling the Signal Conditioners or the Front Panel Assembly, care should be taken not to bend the connector pins.

2. When reconnecting the top and bottom case halves, ensure that the Front and Rear Panels fit into their appropriate grooves in the case top half. Slide the top half into place uniformly. Firmly squeeze top and bottom together (at front and rear), and reinstall the six securing screws.

NOTE

Proper RFI shielding depends on top and bottom case halves being securely mated.

4-11. Input Power

4-12. Input line power voltage is selected by positioning the two switches found in the right rear corner of the Main PCB. Each switch (S4 and S5) shows a position identifying red or white dot. Line voltage settings identified by dot color are presented in Figure 4-2. Factory line voltage settings are identified on the instruments's rear panel; one of four (4) white dots will be darkened to signify 100, 120, 220 or 240V selection.

4-13. Fuse Replacement

WARNING

DISCONNECT THE INSTRUMENT FROM LINE POWER BEFORE ATTEMPTING FUSE REPLACEMENT.

4-14. The 7260A line power fuse is accessible on the rear panel. Fuse requirements are a 3/8A MDL (slo-blo) for line inputs of 100V or 120V and a 3/16A MDL (slo-blo) for line inputs of 220V or 240V.

4-15. To ensure protection from fire, Channel A and Channel B inputs are fused for maximum inputs of 250 mA. Replacement of either signal input fuse necessitates removal of the Main PCB Assembly and the Front Panel PCB Assembly; refer to Instrument Disassembly for removal instructions. Each fuse is soldered to the Front Panel PCB Assembly immediately below the respective BNC input connector. Replacement fuses should be ordered from John Fluke Mfg. Co., Inc.

CAUTION

For protection against fire, replace either signal input fuse with 1/4A, 250V fuse only.

4-16. Cleaning

4-17. Clean the instrument periodicallly to remove dust, grease and other contamination. Use the following procedure:

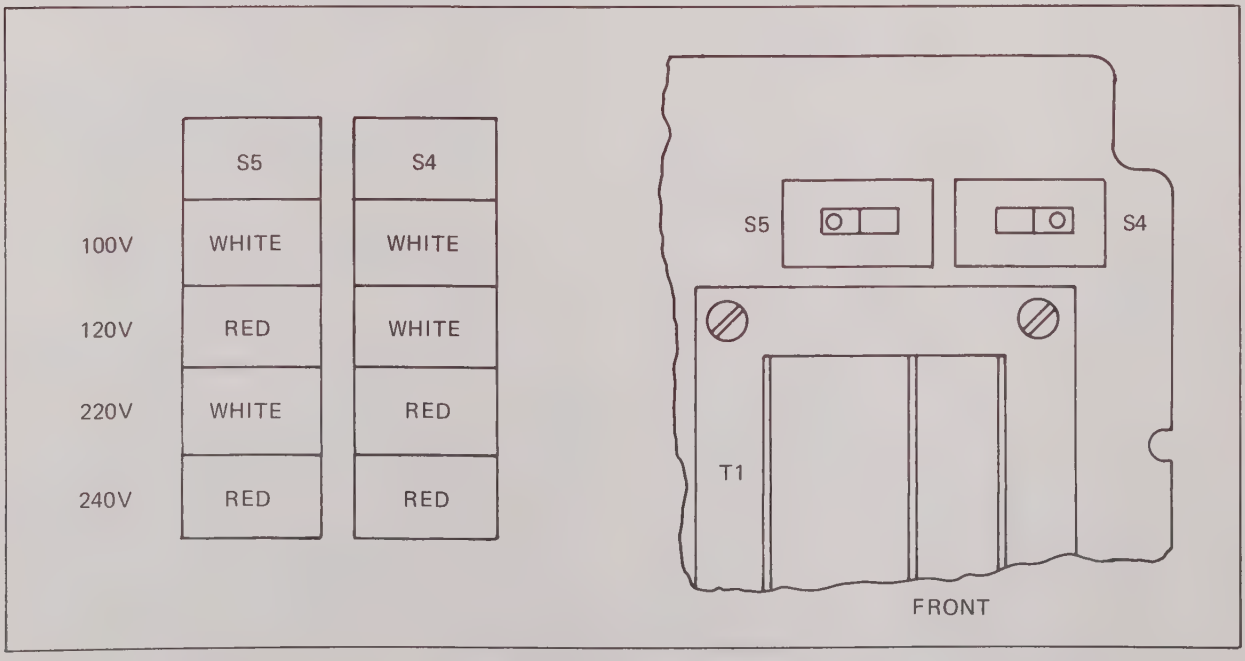


Figure 4-2. Line Voltage Selection

CAUTION

Do not use aromatic hydrocarbons or chlorinated solvents for cleaning. They will react with plastic materials used in manufacture of the instrument.

1. Clean the front panel and case with a soft cloth dampened with a mild solution of detergent and water.

2. Clean the surface of the PCB using clean, dry air at low pressure (≤20 psi). If grease is encountered, spray with Freon T.F. Degreaser or anhydrous alcohol and remove grime with clean, dry air at low pressure.

4-18. Static Discharge Precautions

4-19. Static discharge can damage MOS type integrated circuits found in the 7260A. A list of such components is presented in Table 4-2. The following precautions should be observed when conducting adjustments or repairs with the instrument's top cover removed.

1. Never conduct repairs without first pressing power to STBY and disconnecting the line power cord.

2. Perform all repairs at a static-free work station.

3. Minimize handling of IC's and pcb's; in no case handle them by their connectors.

4. Keep repair parts in their original containers until ready for use.

5. Use static ground straps to discharge repair personnel.

6. Use conductive foam or anti-static containers to store replacement or removed IC's.

7. Remove all plastic, vinyl and styrofoam products from the work area.

8. Do not slide static sensitive devices over any surface.

9. Use only anti-static type solder removal tools.

10. Use grounded tip soldering irons.

Table 4-2. MOS Type Integrated Circuits

ASSEMBLY NAME	REF	TYPE
Main PCB	U12	Custom
Main PCB	U13	LS7031
Main PCB	U31	4511BE

4-20. Soldering Techniques

CAUTION

The Main and Front Panel PCBs are multilayer boards. Irreparable damage may be caused by careless removal or resoldering of components.

4-21. The following board repair procedures are recommended by the John Fluke Mfg. Co., Inc.

1. Restrict soldering iron tip temperatures to 700° F.

2. Use a heat regulated soldering iron.

3. Use the compressed air driven vacuum type of desoldering tool.

4. Do not reheat the same pin or pad until it has been allowed to cool. Excessive heat build-up can cause board warpage, separation of inner board layers, and loss of pads and through-hole connections.

5. Use the following procedure for IC removal:

   a. Cut all pins.

   b. Gently remove the pins by heating the associated solder joint. (Always work in one direction around the IC to allow previously heated pins and pads to cool.)

   c. After the pins are removed, use the vacuum desolderer to remove the remaining solder. Enough heat must be applied to melt the solder completely before suction is employed.

   d. If a small amount of solder remains and cannot be melted, resolder the hole. Allow the solder to cool. Repeat desoldering.

4-22. SELECTED COMPONENT REPLACEMENT

4-23. Each Signal Conditioner Assembly is matched with a selected hysteresis resistor. This resistor, mounted on the Main PCB, is designated R4 for Channel A and R3 for Channel B. If a replacement Signal Conditioner is accompanied with a resistor differing in value from the one already installed, the new resistor must be substituted. Utilize soldering techniques described in this section.

4-24. PERFORMANCE CHECKS

4-25. The Performance Checks are used to compare the performance of the instrument with the Specifications given in Section 1. The Performance Checks are recommended for incoming inspection, maintenance, evaluation after repair, or as an aid in troubleshooting. All of the Performance Checks other than the Time Base Check should be performed quarterly. The Time Base Check should be performed monthly if operation within the Section 1 Specifications is desired. Should the instrument fail any portion of the Performance Checks, calibration and/or repair is indicated. Refer to Table 4-1 when specific test equipment is called for.

NOTE

Read each Performance Test or Calibration procedure through thoroughly prior to actually administering them.

4-26. Initial Preparation

4-27. The following controls should be in the indicated positions prior to conducting any Performance Test.

1. On the Rear Panel of the 7260A, set the controls to the following position:

ON/OFF - ON
INT/EXT - INT
CONT/TRIG - CONT

Line cord connected to line power.

2. On the Front Panel of the 7260A, set the controls to the following position:

ON/STBY - ON
BAT/LINE - LINE
TI HOLDOFF - OFF
RESOLUTION - AUTO
SEP/COM - SEP
FILTER IN/OUT - OUT
TRIGGER LEVEL (A&B) - PRESET
ATTN (A&B) - X1
AC/DC (A&B) - AC
± (A&B) - –

4-28. Sensitivity Test, Channel A

4-29. Use the following procedure to verify that Channel A circuitry meets the sensitivity specifications listed in Section 1.

1. On the 7260A make the following changes to "Initial Preparation":

FUNCTION - FREQ A
RESOLUTION - 1 Hz

2. Connect the 7260A and test equipment as illustrated in Figure 4-3 (part A).

3. Set the low frequency synthesizer for a 10 Hz output at 100 mV rms.

4. Verify a 7260A display of 0.010 kHz (±1 count, ±time base error).

5. Reduce the input level to 10 mV rms and verify a similar, stable display.

6. Repeat steps 3, 4 and 5 at frequencies of 1 kHz, 1 MHz and 10 MHz.

7. Disconnect the low frequency synthesizer, and connect the high frequency synthesizer as illustrated in Figure 4-3 (part B).

8. Set the high frequency synthesizer for an output of 50 MHz at 100 mV rms.

9. Verify a 7260A display of 50000.000 kHz (±1 count, ±time base error).

10. Reduce the input level to 15 mV rms and verify the same, stable display.

11. Set the RESOLUTION control (7260A) to 10 kHz.

12. Repeat steps 8, 9 and 10 at a frequency of 100 MHz.

13. Set the input to 125 MHz at 100 mV rms.

14. Verify a display of 125000.00 kHz.

15. Reduce the input level to 35 mV rms and verify a stable display.

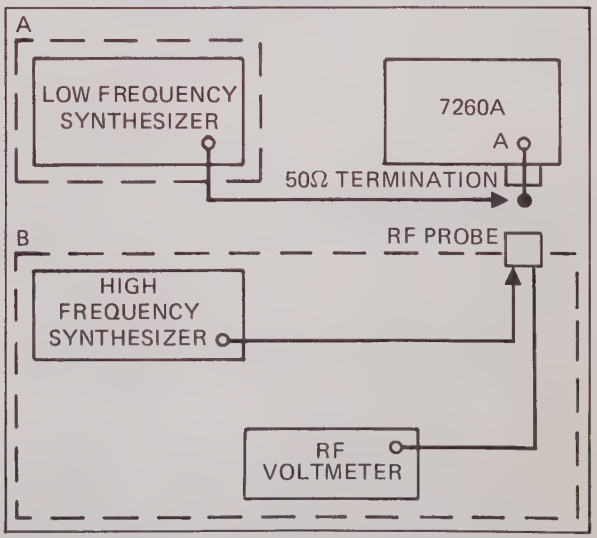


Figure 4-3. Channel A Sensitivity Test

4-30. Sensitivity Test, Channel B

4-31. Use the following procedure to verify that Channel B meets the sensitivity specifications listed in Section 1.

1. Make the following control change to "Initial Preparation":

FUNCTION - RATIO A/B
RESOLUTION - 10°

2. Connect the 7260A and test equipment as illustrated in Figure 4-4.

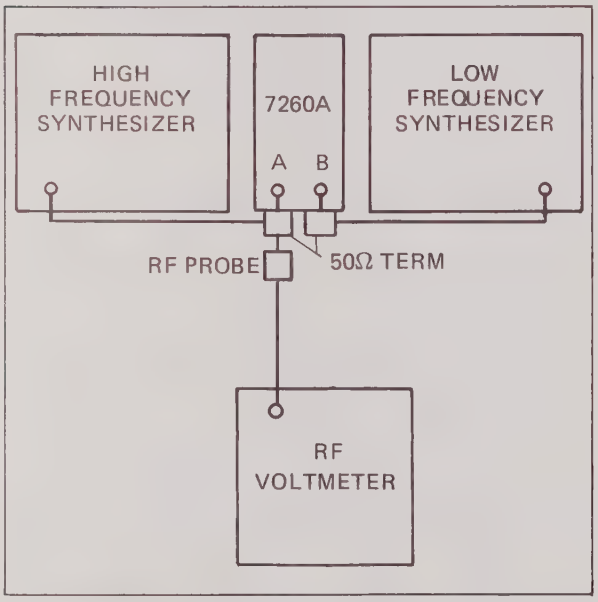


Figure 4-4. Channel B Sensitivity Test

3. Set the high frequency synthesizer for an output of 10 MHz at 100 mV rms.

4. Set the low frequency synthesizer for an output of 10 Hz at 100 mV rms.

5. Verify a display of 1000000, with no units annunciator.

6. Reduce the low frequency synthesizer level to 10 mV rms and verify a similar display.

7. Repeat steps 4, 5 and 6 at Channel B frequencies of 1 kHz, 1 MHz and 2 MHz. Verify a display of 10000, 10, and 5 respectively.

4-32. Time Base Test

4-33. Use the following procedure to check the accuracy of the time base and the operation of the REF OUT circuitry.

1. On the 7260A, set the Front Panel controls as follows:

FUNCTION - FREQ A
RESOLUTION - .1 Hz
ON/STBY - ON

2. Connect the LF synthesizer to the Channel A input terminal of the 7260A via a 50Ω termination and the shortest length of RG-58 cable possible.

3. Set the LF synthesizer for an output of 5 MHz at a level of 100 mV.

4. Verify, on the 7260A, that the display reading is 5 MHz ± maximum allowable count error. Table 4-3 lists the maximum allowable count error at 5 MHz

Table 4-3. Time Base Performance Check

TIME BASE TYPE	FREE AIR	TCXO OPTION -112	OVEN OPTION -131	OVEN OPTION -132
Total Time Base Accuracy *	+/–56 X 10^{-7}	+/–23.2 X 10^{-7}	2.2 X 10^{-7}	8.4 X 10^{-8}
Maximum Allowable Deviation ** (with 5 MHz input)	+/–28.0 Hz	+/–11.6 Hz	+/–1.1 Hz	+/–0.5 Hz

* Includes aging rate, temperature effects, line voltage variation.
** Allowable deviation in Hz is found by multiplying the input frequency (5 MHz in this case) by the total accuracy, and adding 1 count error. These figures apply when in 0.1 Hz RESOLUTION.

for each of the four time bases available for use with the instrument. The maximum allowable count error can be computed for any input signal by multiplying the frequency of the input signal by the total time base accuracy (given in Table 4-3) and adding the ±1 count to the product.

5. Connect the oscilloscope to the REF OUT terminal on the 7260A through as short a length of RG-58 as possible. The oscilloscope end of the test cable must have a 50Ω termination.

6. Verify that the signal displayed on the oscilloscope is a 10 MHz, 500 mV p-p waveform.

4-34. Display Test

4-35. The following procedures will verify proper decimal point placement, measurement unit annunciation and scaling factor operation without an input signal. To verify individual display digit operation, perform "Totalize Test".

1. Complete Initial Preparation. Ensure that Channel A and B inputs are disconnected.

2. Place the FUNCTION control in FREQ A. Verify that the display digits and measurement unit annunciators appear as defined in Table 4-4 for each RESOLUTION setting.

NOTE
RESET the 7260A after each check in AUTO.

3. Place the FUNCTION control in CPM X100A. On all RESOLUTION settings, the measurement units annunciators should be blank, and the display should read: 0.

4. Sequence the FUNCTION control through each of the next six positions. Verify correct display digit placement and measurement unit annunciation per Table 4-4.

5. Select TOT A with the FUNCTION control. The measurement unit should now be blank and the display should read: 0 (all RESOLUTION settings).

6. Set the FUNCTION control to CHK: verify that display indications match those of Table 4-4. Also check that the display reads "88888888" when the RESET switch is held depressed (all RESOLUTION settings).

4-36. Frequency A Function Test

4-37. Procedures for checking the 7260A during frequency measurements on Channel A are covered under "Sensitivity Test, Channel A".

4-38. Frequency C Function Test

4-39. Verifying procedures for Channel C frequency measurements necessitate an installed Channel C option. These procedures are covered in Section 6.

4-40. Counts Per Minute Function Test

4-41. Use the following method for testing for proper operation of the 7260A during CPM X100A measurement:

1. Make the following changes to "Initial Preparation":

FUNCTION - CPM X100A
RESOLUTION - 10 kHz

2. Apply a 1 MHz, 10 mV rms signal from the low frequency synthesizer to Channel A input, as illustrated in Figure 4-3 (part A).

3. Verify a display of 600000 with no decimal point or units annunciator.

4. Change the RESOLUTION control on the 7260A successively through the remaining settings and verify that no aspect of the display changes.

4-42. Ratio A/B Function Test

4-43. Procedures for verifying ratio measurements are covered under "Sensitivity Test, Channel B".

4-44. Period A Function Test

4-45. Use the following procedure to verify proper 7260A operation in the period measuring function:

1. Make the following change to "Initial Preparation":

FUNCTION - PER A
RESOLUTION - 100 ns

2. Connect the 7260A and test equipment as illustrated in Figure 4-3 (part A).

3. Set the low frequency synthesizer for an output of 1 kHz at 100 mV rms.

4. Verify a stable display on the 7260A of 1.0000 msec (±synthesizer instability).

5. Set the low frequency synthesizer for an output of 2 MHz at 100 mV rms.

6. Verify a 7260A display of 0.0005 msec.

Table 4-4. Display Test

FUNCTION	RESOLUTION SWITCH	DIGIT DISPLAY	UNITS ANNUNCIATOR
FREQ A	10 kHz	0.00	MHz
	1 kHz	0.000	MHz
FREQ C	100 Hz	.0000	MHz
	10 Hz	0.00	kHz
	1 Hz	0.000	kHz
	.1 Hz	0.0000	kHz
	AUTO	0.000	kHz
CPM X100A	All settings	0	Blank
RATIO A/B	10^0	0	Blank
	10^1	0.0	Blank
	10^2	0.00	Blank
	10^3	0.000	Blank
	10^4	0.0000	Blank
	10^5	0.00000	Blank
	AUTO	0	Blank
PER A	100 ns	0.0000	msec
	1 μs	0.000	msec
	10 μs	0.00	msec
TI A-B	100 μs	0.0000	sec
	1 ms	0.000	sec
	10 ms	0.00	sec
	AUTO	0.00	msec
PER AVG A	10^0	0.0000	msec
	10^1	0.00000	msec
	10^2	0.000	μsec
TIA A-B	10^3	0.0000	μsec
	10^4	0.00000	μsec
	10^5	0.000000	μsec
	AUTO	0.0000	msec
TOT A-B	All settings	0	Blank
CHK	10 kHz	10.00	MHz
	1 kHz	10.000	MHz
	100 Hz	10.0000	MHz
	10 Hz	10000.00	kHz
	1 Hz	10000.000	kHz
	.1 Hz	*0000.0000	kHz
	AUTO	10000.00	kHz

*OVFL annunciator turns on after 10 sec gate time

4-46. Period Average A Function Test

4-47. Use the following procedure to test for proper 7260A operation during period averaging measurements:

1. Make the following front panel control changes to "Initial Preparation":

FUNCTION - PER AVG A
RESOLUTION -10^0

2. Connect the 7260A and test equipment as illustrated in Figure 4-3 (part A).

3. Set the low frequency synthesizer for an output of 10 kHz at 100 mV rms.

4. Verify a stable display on the 7260A of 0.1000 msec.

5. Set the 7260A RESOLUTION control to 10^5.

6. Set the low frequency synthesizer for an output of 2 MHz at 100 mV rms.

7. Verify a 7260A display of 0.500000 μsec.

4-48. TI A-B Function Test

4-49. Use the following procedure to verify 7260A operation during time interval measurements:

1. Make the following front panel control changes to the "Initial Preparation":

FUNCTION - TI A-B
RESOLUTION - 100 nsec
SEP/COM - COM
ATTEN (A) - X100

2. Connect the low frequency synthesizer TTL output to the 7260A as illustrated in Figure 4-3 (part A).

3. Set the low frequency synthesizer for 10 kHz.

4. Set the CHANNEL A and B slope controls (+/–) and observe the display as defined in Table 4-5.

5. Turn the front panel TI Holdoff control on, but fully ccw against the switch detent. The display should be 0.1000 msec.

6. Set the low frequency synthesizer to 1 MHz; the display should be 0.0010 msec or less.

7. Make the following front panel control changes:

RESOLUTION - 1 kHz
TI Holdoff - fully cw

8. The display should be 25 msec or greater.

Table 4-5. Time Interval Test

SLOPE A	SLOPE B	DISPLAY
–	–	xxx0.1000 msec
+	–	xxx0.0500 "
–	+	xxx0.0500 "
+	+	xxx0.1000 "

4-50. Time Interval Average Function Test

4-51. Use the following procedure to verify 7260A operation during the TIA A-B mode:

1. Make the following change to "Initial Preparation":

FUNCTION - TIA A-B
RESOLUTION - 10^0
Slope controls - (+) (Channels A and B)
REF (Rear Panel) - EXT

2. Connect the 7260A and test equipment as illustrated in Figure 4-5.

3. Set the low frequency synthesizer for an output of 1.12345 MHz at 2.0V rms.

4. The display should be 0.0004 msec.

5. Verify display stability for at least 10 samples at each RESOLUTION setting, as indicated in Table 4-6.

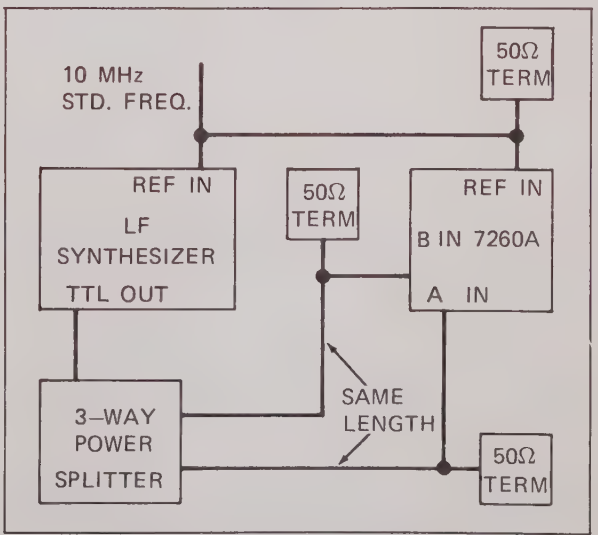


Figure 4-5. Time Interval Average Test

Table 4-6. Time Interval Average Test

RESOLUTION	DISPLAY	STABILITY (+/– counts)
10^0	0.0004 msec	±1
10^1	0.00044 msec	±3
10^2	0.445 μsec	±10
10^3	0.4450 μsec	±33
10^4	0.44505 μsec	±100
10^5	0.445055 μsec	±330

4-52. Totalize A Function Test

4-53. The following procedure may be used to verify 7260A operation during totalize measurements and to verify proper operation of each display digit segment.

1. On the 7260A front panel, make the following changes to basic control settings listed in "Initial Preparation":

FUNCTION - TOT A B
AC-DC (A and B) - DC
Slope (±) - + (both channels)
TRIGGER LEVEL A - fully clockwise
TRIGGER LEVEL B - counterclockwise, but not on PRESET

2. Ensure that input signals to both channels are disconnected. The GATE LED should be lit.

3. Depress the RESET control and observe that the display resets to 0.

4. Rotate TRIGGER LEVEL A fully cw, but not to PRESET, and then back to the cw position. As the trigger status LEDs shift from (+) to (–), the display should update by one count. Repeat this procedure through a displayed count of 10.

5. Connect the low frequency synthesizer to the 7260A at CHANNEL A input. Set TRIGGER LEVEL A to PRESET.

6. Set the synthesizer for a 10 Hz output at 100 mV rms. Observe that digit 2 in the display is sequencing properly and that all segments are operating.

7. Check each of the remaining six digits in a similar manner. Use frequencies of 100 Hz for digit 3, 1 kHz for digit 4, 10 kHz for digit 5, 100 kHz for digit 6, 1 MHz for digit 7 and 10 MHz for digit 8.

8. Rotate TRIGGER LEVEL B fully cw; the trigger status (–) LED should come on. The GATE LED should go off and the count sequence should stop.

4-54. Self Check Function Test

4-55. Use the following procedure to verify 7260A operation in the CHK mode.

1. Make the following change to the "Initial Preparation":

FUNCTION - CHK
RESOLUTION - 1 Hz

2. The display should be 10000.000 kHz (±1).

3. Change the RESOLUTION to 10 kHz and verify a display of 10.00 MHz. The GATE LED should be flashing approximately 5 times per second.

4. Depress the RESET control. The display should be 888888.88 MHz and gating should cease for as long as the control is held depressed.

4-56. Autoranging Test

4-57. Use the following procedure to verify correct operation of the 7260A autoranging circuitry:

1. Make the following changes to "Initial Preparation":

FUNCTION - FREQ A
AC/DC - DC

2. Connect the low frequency synthesizer to Channel A input. Set the output for 100 Hz at 100 mV rms.

3. Verify a display of 0.100 kHz.

4. Change the output to 10 MHz and observe a display of 10000.00 kHz.

5. Change the output to 2 MHz at 100 mV rms.

6. Change FUNCTION to PER AVG A.

7. Verify a display of 0.50000 msec.

8. Change the low frequency synthesizer output to 100 Hz at 100 mV rms.

9. Verify a display of 10.00000 msec.

4-58. Filter Test

4-59. Use the following procedure to verify operation of the 100 kHz low pass filter:

1. Make the following change to the "Initital Preparation":

FUNCTION - FREQ A
RESOLUTION - 1 Hz

2. Connect the low frequency synthesizer to Channel A input. Set the output for 1 MHz at 10 mV rms.

3. Verify that the display reads 1000.000 kHz.

4. Switch the FILTER control to IN; verify a display of 0.000 kHz.

5. Increase the signal level until the display again reads 1000.000 kHz. Verify that the input signal level is greater than 100 mV rms.

4-60. External Reference Input Test

4-61. Use the following procedure to test 7260A performance with an external reference input used as the time base:

1. Make the following changes to "Initial Preparation":

FUNCTION - FREQ A
RESOLUTION - 10 Hz
REF (rear panel) - EXT

2. Connect the 7260A and test equipment as illustrated in Figure 4-6.

3. Set the low frequency synthesizer for an output of 10 MHz at 300 mV rms.

4. Set the high frequency synthesizer for an output of 100 MHz at 100 mV rms.

5. Verify a display on the 7260A of 100000.00 kHz.

6. Increase the high frequency synthesizer input by first 100 Hz, then by 200 Hz. Verify that the display changes accordingly.

7. Set the REF control on the rear panel to INT.

8. Repeat steps 4, 5, and 6.

4-62. Reference Output Test

4-63. Connect an oscilloscope to the rear panel 10 MHz REF OUT connector and verify a 10 MHz TTL waveform (≥.5V into 50Ω).

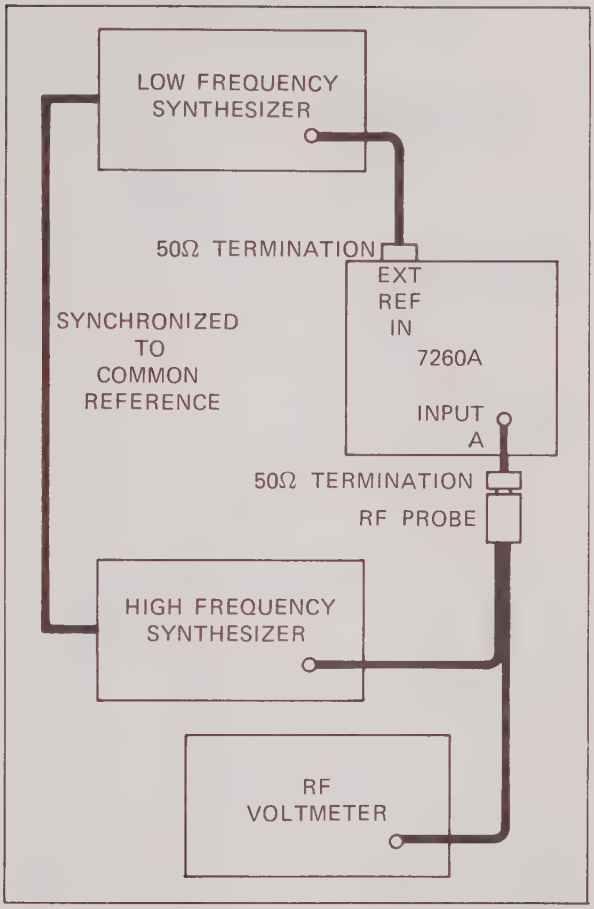


Figure 4-6. External Reference Input Test

4-64. Marker Output Test

4-65. Use the following procedure to confirm proper marker outputs:

1. Make the following change to "Initial Preparation":

FUNCTION - TI A-B
RESOLUTION - 100 ns
SEP/COM - COM

2. Connect the 7260A and test equipment as portrayed in Figure 4-7.

3. Set the low frequency synthesizer for an output of 1 kHz at 1.5V rms.

4. Use the front panel slope and TRIGGER LEVEL controls for each setting listed in Table 4-7. Appropriate waveforms, as listed is Table 4-7, are illustrated in Figure 4-8.

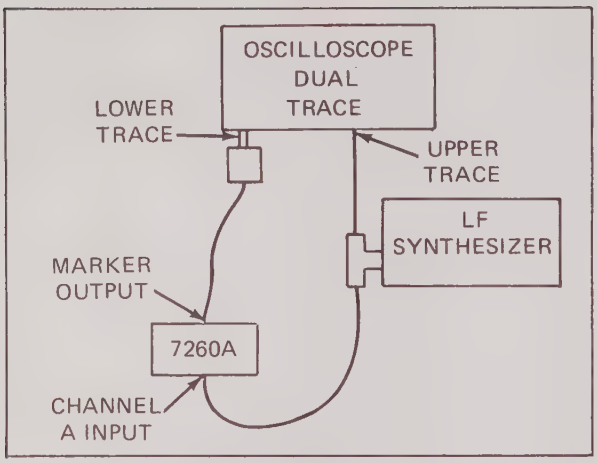


Figure 4-7. Marker Check

Table 4-7. Marker Output Test Settings

SLOPE		TRIGGER LEVEL		OUTPUT WAVE-FORM
A	B	A	B	
+	–	CW	CCW	1
–	+	CW	CCW	2
+	–	CCW	CW	3
–	+	CCW	CW	4
+	–	PRESET	PRESET	5
–	+	PRESET	PRESET	6

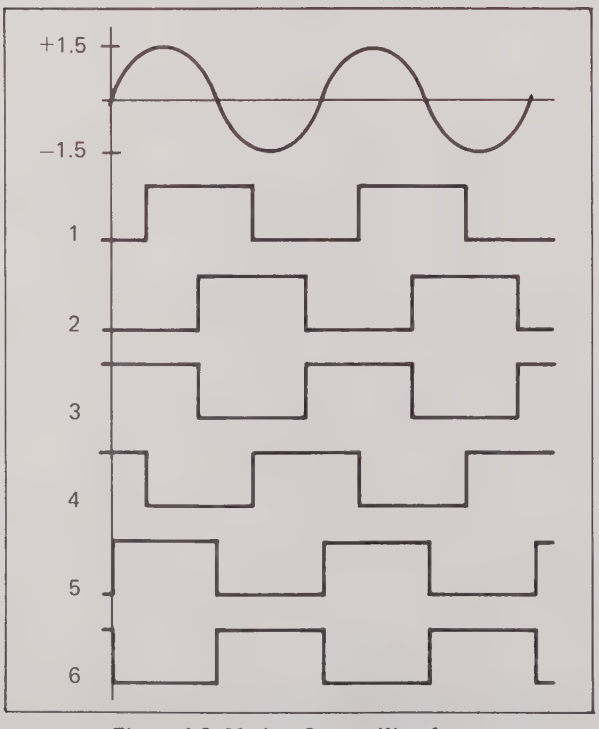


Figure 4-8. Marker Output Waveforms

4-66. Trigger Mode Test

4-67. Use the following procedure to verify instrument operation in the single trigger mode:

1. Make the following change to "Initial Preparation":

FUNCTION - FREQ A
RESOLUTION - 1 Hz
Slope (Channel A) - +
Slope (Channel B) - –
CONT/TRIG - TRIG

2. Press RESET, and observe a display of 0.000 kHz without a GATE indication.

3. Change the Channel B Slope control to (+), and observe that the 7260A gates once for a display of 10000.000 kHz.

4. Return the CONT/TRIG control to CONT. The GATE LED should be flashing.

4-68. CALIBRATION

4-69. Calibration for the 7260A consists of Time Base and trigger level adjustments. These adjustments should be made after repairs are completed or whenever the instrument fails to meet PERFORMANCE TEST requirements.

4-70. Time Base Calibration

4-71. Calibration should be made whenever the time base is repaired or replaced, or when it is determined that instrument accuracy is not within the accuracy desired. The Time Base Accuracy Test can be used as an intitial accuracy determination. Calibration adjustments for optional time bases (-112, -131, -132 models) are included in Section 6. Perform the Time Base adjustment in an environment having an ambient temperature between 20°C and 30°C (68°F to 86°F). Use the following procedure when calibrating the time base:

1. Connect the 7260A and the low frequency synthesizer as illustrated in Figure 4-3 (part A). Use a 50Ω termination at the Channel A input and as short a length of coaxial cable as possible (RG-58 recommended).

2. Allow the 7260A to operate for at least 5 minutes with both covers on before proceeding.

3. On the 7260A, make the following changes to "Initial Preparation":

FUNCTION - FREQ A
RESOLUTION - 1 Hz
AC/DC - DC (Channel A)
Slope - + (Channel A)

4. Set the low frequency synthesizer for an output of 10 MHz at 100 mV rms.

5. Verify a 7260A display near 10000.000 kHz. If necessary, use a JFD 5284, or equivalent, non-ferrous tuning tool to adjust the time base for the indicated display. Adjust for a display as close as possible to the optimum 10000.000 kHz. Figure 4-9 shows the location of the time base adjustment access in the bottom case half of the 7260A.

6. On the 7260A front panel, change the RESOLUTION setting to 0.1 Hz.

7. Any display update will now take 10 seconds. The OVFL LED will come on after the initial 10 seconds if 10 MHz or more are counted.

NOTE

Verify that a measurement is in progress by observing both the OVFL and GATE LEDs illuminated.

8. Adjust the time base, allowing for the 10 second display update, until the display reads as close as possible to 0000.0000 (OVFL) or between a lower limit of 9999.9449 and an upper limit of 0000.0551 (OVFL).

9. If adjustment does not yield a display within these limits, disconnect the 7260A's line power cord, remove the top case half and look at the top of the time base pcb (left rear corner of Main PCB). For some versions of the Free Air Time Base, another coarse adjustment is included here. If your instrument is so equipped, perform "Coarse Time Base Adjustment".

10. If the time base cannot be adjusted within specifications and coarse adjustment is not available, refer to TROUBLESHOOTING.

11. After 24 hours, recheck any adjustment performed to verify stability.

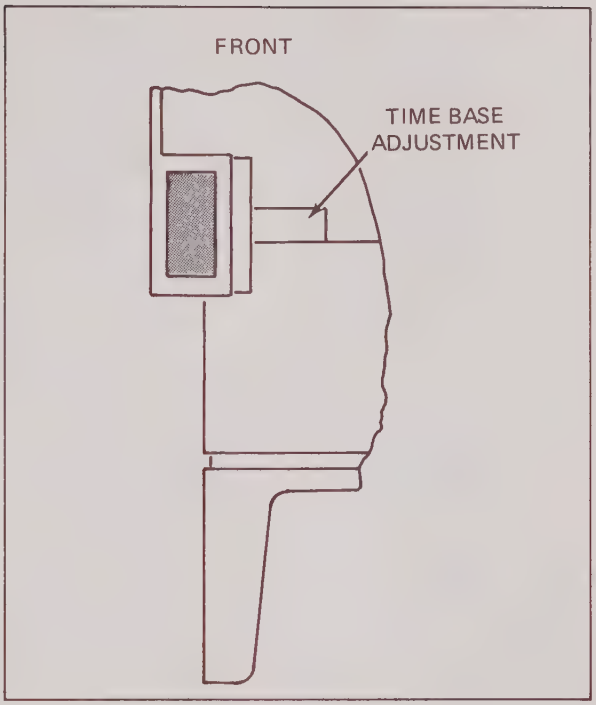


Figure 4-9. Time Base Adjustment Location

4-72. Coarse Time Base Adjustment

4-73. Some versions of the Free Air Time Base will have an additional coarse adjustment control. This control is located on top of the time base and is accessible only with the 7260A's top case half removed.

NOTE

Do not perform coarse adjustment unless the Time Base Calibration procedure fails to bring the instruments within the specifications.

If coarse adjustment is determined necessary, use the following procedure:

1. Set the fine adjustment, accessed through the bottom case half, to mid-range.

2. Remove the instrument's top cover (see Disassembly).

3. Perform steps 2, 3 and 4 of Time Base adjustment.

4. Use a non-ferrous alignment tool adjust the coarse control for a display as close as possible to 10000.000 kHz.

5. Replace the top case half (see Reassembly) and perform Time Base Calibration.

4-74. Trigger Level Adjust, Channel A

4-75. Use the following procedure when adjusting the Channel A trigger level:

1. Make the following changes to "Initial Preparation":

FUNCTION - FREQ A
RESOLUTION - 1 Hz
Slope - + (Channel A)

2. Connect the 7260A and test equipment as illustrated in Figure 4-4.

3. Set the high frequency synthesizer for a 10 MHz output at 10 mV rms.

4. Connect an oscilloscope to U6-3 on the 7260A Main PCB.

5. If necessary, adjust R12 for a 50% duty cycle TTL waveform.

6. Disconnect the oscilloscope.

7. Set the high frequency synthesizer for an output of 125 MHz at 10 mV rms.

8. Observe the display (125 MHz in overflow) for stability. If necessary, slightly adjust R12 to obtain stability.

4-76. Trigger Level Adjustment, Channel B

4-77. Use the following procedure when adjusting the Channel B trigger level.

1. Make the following changes to "Initial Preparation":

FUNCTION - RATIO A/B
RESOLUTION - 0.1 Hz
Slope - + (Channels A and B)

2. Connect the 7260A and test equipment as illustrated in Figure 4-4.

3. Set the low frequency synthesizer for a 2 MHz output at 10 mV rms.

4. Connect an oscilloscope to U6-6 on the 7260A Main PCB.

5. If necessary, adjust R2 to obtain a 50% duty cycle TTL waveform.

6. Disconnect the oscilloscope.

7. Set the low frequency synthesizer for a 1 MHz output at 10 mV rms.

8. Set the high frequency synthesizer for a 125 MHz output at 10 mV rms.

9. Observe the display 125.00000 for stability. If necessary, adjust R2 slightly to obtain stability.

4-78. TROUBLESHOOTING

4-79. Introduction

4-80. The material in the remainder of this section is presented as a troubleshooting aid for the technician. If the instrument fails to perform as expected, select the CHK function. If the instrument display is incorrect, the fault is in the instrument; if the display is correct, the fault may not lie in the instrument. Ask the following questions before proceeding any further:

1. Are the instrument controls set to the proper position?

2. Are the controls of associated equipment set to the proper positions?

3. Are the connections between the instrument and associated equipment correct?

4. Are the interconnecting cables in working order?

5. Is the associated equipment functioning properly?

6. Is the instrument designed to do what is being attempted?

If the answers to these questions are all "yes", then the fault is probably in the instrument.

4-81. The ease with which a technician isolates a fault in any instrument depends primarily upon just how well that technician knows the instrument. Sections 2 and 3 of this manual should be read and thoroughly understood before attempting to troubleshoot. As an aid to the troubleshooter, three additional subsections follow: Visual Inspection, Fault Isolation Guide, and Troubleshooting Techniques. The Visual Inspection should be performed first. The Fault Isolation Guide is a brief check of all instrument functions. This procedure should enable the technician to isolate the fault to a particular circuit or group of circuits. Once a suspect circuit is identified, the Troubleshooting Techniques provide the technician with suggestions for troubleshooting IC technology circuits.

4-82. Whenever working with the instrument, heed techniques presented in this section for handling components and preventing static discharge damage. Care should especially be taken when soldering, as obvious (and hidden) damage to the instrument may result.

4-83. The instrument uses three basic types of logic: ECL, TTL, and CMOS. The circuits handling high frequency signals employ Emitter Coupled Logic (ECL). Circuitry using CMOS IC's operate at CMOS logic levels. The remainder of the instrument employs Transistor-Transistor Logic (TTL). Table 4-8 lists typical high and low logic levels for each logic type. Refer to the Maintenance Locator drawing (Figure 4-10) for adjustment and test point locations.

Table 4-8. Typical Logic Levels

	LOGIC 1	LOGIC 0
TTL	2.5V	0.6V
ECL	4.1V	3.2V
CMOS	>3.5V (>70% of supply)	<1.5V (<30% of supply)

4-84. Visual Inspection

4-85. Visual inspection can sometimes quickly locate instrument faults saving the technician the time usually consumed in extensive troubleshooting. Use the Disassembly procedure presented earlier in this section to remove the top case cover. Carefully inspect the instrument inside and out. Check for loose or broken wires and component leads, improperly seated plug-in assemblies, physically damaged components, discoloration due to arcing, etc. Shorted IC's usually have a small bubble or discoloration at the center of the package. Shorted capacitors or resistors in short paths are often discolored or burnt. Abusively high overloads may blow carbon composition resistors, glass diodes, ceramic capacitors, thermistors, etc. into fragments. These symptoms or anything that looks suspect should be carefully checked before proceeding with involved troubleshooting.

4-86. Fault Isolation Guide

4-87. The Fault Isolation Guide is a simplified check of instrument performance. It is intended to direct the troubleshooter to the defective circuit or circuits. There are three basic cases of improper operation:

1. The instrument will not turn on. Use the Power ON procedure.

2. The instrument turns on but the problems seem to be spread thoughout the instrument or are erratic. This situation may be due to any of a number of power supply related problems. Use the Power On procedure.

3. The instrument has a problem in one or more function or range. Use the Improper Operation procedure.

4-88. POWER ON PROCEDURE

CAUTION

Line power voltage is present from the power cord throughout the primary circuit or the main power transformer. Do not contact this voltage.

4-89. If the instrument cannot be turned on, the problem may lie in several areas: the line power used may not be present, the AC POWER switch may be in the OFF position, the main power fuse, F1, may be blown, or there may be a power supply problem. Power supply problems can be caused both by faults in the power supply circuitry and by shorts in the instrument loading down the power supply. Points to consider when attempting to isolate power supply problems are listed below. If the 7260A will operate but the symptoms are erratic, widespread or seemingly disassociated, then proceed directly to item number 6.

1. Insure that line power is present at the receptacle being used.

2. Insure that the Rear Panel AC POWER switch is in the ON position.

3. Disconnect the line power cord and check F1, (the main power fuse).

4. Make continuity measurements between chassis common and the three pins of the power receptacle. The ground pin to common should be zero ohms. The other two pins to common should be infinity.

5. Make the continuity measurement between the two non-ground pins of the Rear Panel power receptacle. (The AC POWER switch should be in the ON position.) There should be some small resistance (the measurement is taken through the primary windings of the main power transformer).

6. Connect the line power cord. Measure the power supply voltages at TP1, TP2, TP3 and TP4 with the Front Panel POWER ON/STBY switch in both positions. Use E1 for the common reference

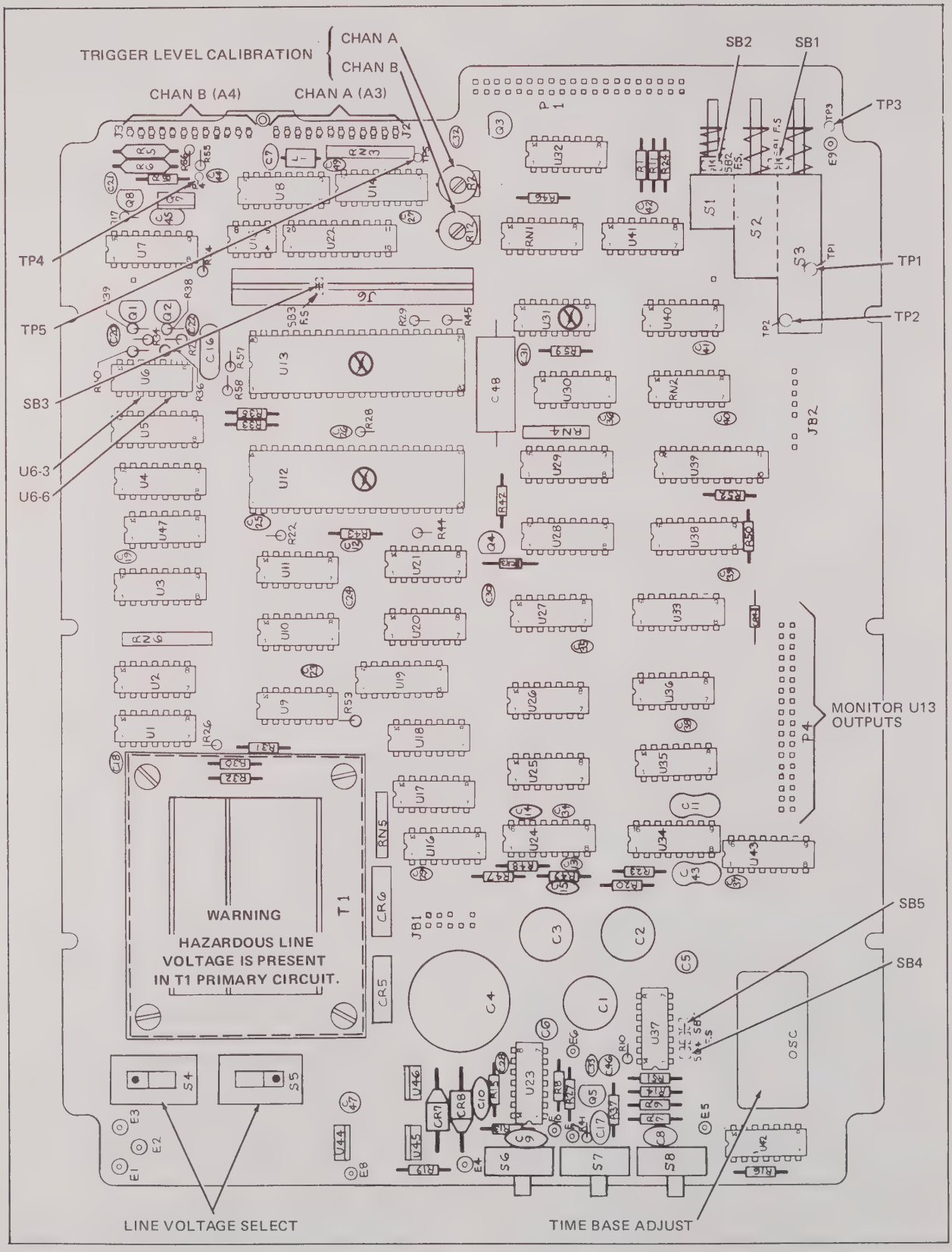


Figure 4-10. Maintenance Locator

when making these measurements. If all voltages are within the limits listed (Table 4-9), proceed to item 7. If one or more voltage is incorrect when the POWER ON/STBY switch is in the STBY position, the problem is in the power supply, proceed to item 6, part a. If one or more voltage is incorrect only when the POWER ON/STBY switch is in the ON position, the fault does not lie in the power supply, proceed to item 6, part b.

a. Problems in the power supply can be tracked down using conventional methods, but remember that:

1) The –5V supply "tracks" the +5V supply so if the +5V supply has a problem, it will affect both power supplies.

2) The –12V and +12V supplies, after rectification, are independent of the other supplies. Problems in all four power supplies indicate that the fault lies in the primary circuit, transformer, or CR1.

b. Shorts that load down a particular power supply can best be isolated by disconnecting the pcbs that plug into the Main PCB, one at a time. Remember to turn the instrument off before disconnecting or connecting cables, plugs or pcbs. If the short cannot be located by unplugging pcbs, use the current probe tracing procedure described in Troubleshooting Techniques. Start at the output of the power supply that is loaded down.

Table 4-9. Power Supply Voltages

TEST POINT	VOLTAGE	TOLERANCE
TP1	+12V	+/–0.5V
TP2	–12V	+/–0.5V
TP3	+5V	+/–0.2V
TP4	–5V	+/–0.2V

4-90. IMPROPER OPERATION PROCEDURE

4-91. The Improper Operation Procedure is a simple dynamic test of the instrument. The procedure provides a speedy overall view that is interpreted by Table 4-10 to guide the technician to the most likely circuits. Additional information can be gained to aid troubleshooting by performing the Performance Checks indicated by the results of the procedure. The 7260A can pass all parts of the procedure and still have faults. Should the 7260A pass the procedure, do the Performance Checks. Use the following steps to perform the Improper Performance Procedures.

1. Set the instrument controls as follows:

RESOLUTION - 1 kHz
SEP/COM - SEP
FILTER - OUT
CHANNEL A & B
  TRIGGER LEVEL - PRESET
  ATTEN - X1
  AC/DC - DC
  ± - +
  REF - INT

2. Connect the LF synthesizer to the Channel A input terminal of the 7260A via a 50Ω termination.

3. Set the LF synthesizer for an output of 1 MHz at a level of 100 mV rms.

4. To check the FREQ A function:

a. Set the FUNCTION control to the FREQ A position.

b. Verify that the GATE annunciator is flashing and that the display is 1.000 MHz.

5. To check the CPM X100A function:

a. Set the FUNCTION control to the CPM X100A position.

b. Verify that the GATE annunciator is flashing and that the display is 600000.

6. To check the FREQ C function: Refer to Section 6.

7. To check the RATIO A/B function:

a. Set the FUNCTION control to the RATIO A/B position.

b. Set the SEP/COM switch to the COM position.

c. Verify that the GATE annunciator is flashing and that the display is 1.0.

d. Set the SEP/COM switch to the SEP position.

8. To check the PER A function:

a. Set the FUNCTION control to the PER A position.

b. Verify that the GATE annunciator is flashing and that the display is 0.001 msec.

c. Set the RESOLUTION control to the 100 ns position.

d. Verify that the GATE annunciator is flashing and that the display is 0.0010 msec. (R0 check.)

9. To check the PER AVG A function:

a. Set the FUNCTION switch to the PER AVG A position.

b. Verify that the GATE annunciator is flashing and the display is 0.0010 msec.

10. To check the TI A-B function:

a. Set the FUNCTION control to the TI A-B position.

b. Set the Channel B ± control to the – position.

c. Place the SEP/COM control in COM.

d. Verify that the GATE annunciator is flashing and that the display is 0.0005 msec.

11. To check the TIA A-B function:

a. Set the FUNCTION control to the TIA A-B position.

b. Verify that the GATE annunciator is flashing and that the display is 0.0005 msec.

12. To check the TOT A B function:

a. Place the SEP/COM switch to the SEP position.

b. Rotate the Channel B TRIGGER LEVEL control just off PRESET, to the fully counterclockwise variable position.

c. Set the FUNCTION control to the TOT A B position.

d. Press and release the RESET control on the 7260A's front panel. The display should read zero.

e. Rotate the Channel B TRIGGER LEVEL control maximum clockwise.

f. Verify that the gate annunciator is on and a count begins to accumulate in the display.

4-92. Troubleshooting Techniques

4-93. Following are listed several techniques useful in isolating a fault in the instrument.

4-94. CURRENT TRACING

4-95. Current Tracer probes, such as the HP 547A, are usually the best way to locate shorts in the instrument. If the short is so bad that the power supply is loaded down, the Performance Checks or Fault Isolation Guide may not provide any help in isolating the faulty circuit. Starting at the output of the loaded power supply, logically move the Current Tracer through the instrument until the short is found. The Current Tracer will glow brightest at the terminal of the shorted gate.

4-96. HEATING AND COOLING

4-97. Alternately warming (with a heat gun) and cooling (with freon spray) of possible faulty circuits provides a fast and effective troubleshooting technique. This method's range of usefulness extends from large areas on a pcb to individual components. For example, a particular power supply voltage can be monitored while successively spraying IC's with freon; a sudden rise in a loaded voltage would indicate a shorted IC.

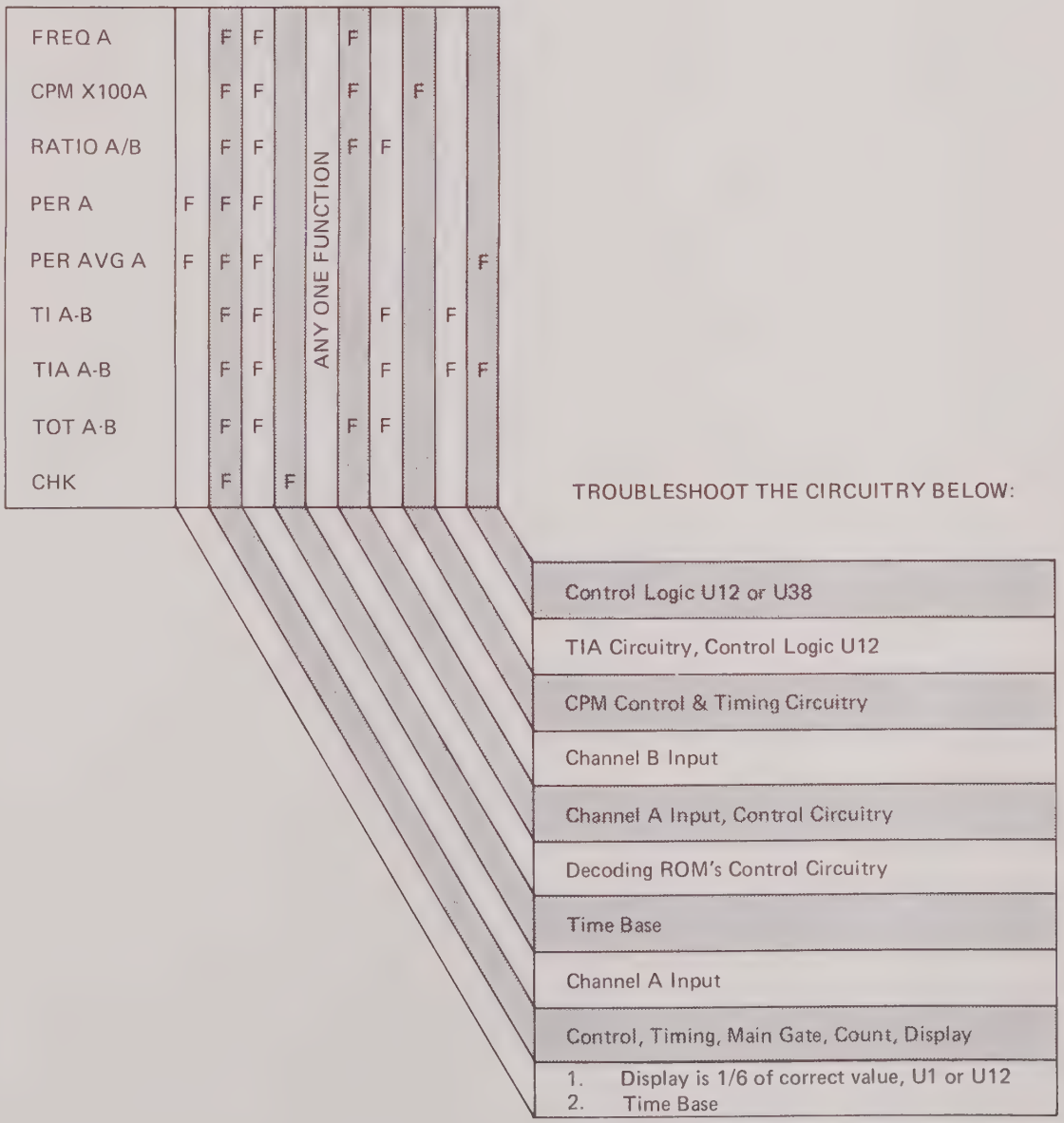
4-98. LOGIC CLIP

4-99. Logic clips, such as the Fluke Testclip 200, provide the troubleshooter with dynamic, visual indication of the logic levels. Since such a device clips onto the IC, it provides for both ease of use and simultaneous observation of inputs and outputs.

4-100. MEASURING TEMPERATURE

4-101. Shorted components overheat. Resulting temperature differences can be monitored with the Fluke 80T-150 and any of its associated digital multimeters.

Table 4-10. Fault Isolation Guide Interpretation



Section 5
List of Replaceable Parts

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A5 Time Base PCB Assembly	5-4	5-17	5-4	5-17

5-1. INTRODUCTION

5-2. This section contains an illustrated parts breakdown of the instrument. A similar parts listing for each of the Options will be found in Section 6. Components are listed alphanumerically by assembly. Both electrical and mechanical components are listed first by reference designation and second by item number. Each listed part is shown in an accompanying illustration.

5-3. Parts lists included the following information:

1. Reference Designation or Item Number.

2. Description of each part.

3. FLUKE Stock Number.

4. Federal Supply Code for Manufacturers. (See Section 7 for Code-to-Name list.)

5. Manufacturer's Part Number or Type.

6. Total Quantity per assembly or component.

7. Recommended Quantity: This entry indicates the recommended number of spare parts necessary to support one to five instruments for a period of two years. This list presumes an availability of common electronic parts at the maintenance site. For maintenance for one year or more at an isolated site, it is recommended that at least one of each assembly in the instrument be stocked. In the case of optional subassemblies, plug-ins, etc., that are not always part of the instrument, or are deviations from the basic instrument model, the REC QTY column lists the recommended quantity of the item in that particular assembly.

5-4. HOW TO OBTAIN PARTS

5-5. Components may be ordered directly from the manufacturer by using the manufacturer's part number, or from the John Fluke Mfg. Co., Inc. factory or authorized representative by using the FLUKE STOCK NUMBER. In the event the part you order has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions if necessary.

5-6. To ensure prompt and efficient handling of your order, include the following information.

1. Quantity.

2. FLUKE Stock Number.

3. Description.

4. Reference Designation or Item Number.

5. Printed Circuit Board Part Number.

6. Instrument Model and Serial Number.

⊗CAUTION
Indicated devices are subject to damage by static discharge.

Table 5-1. Final Assembly

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	FINAL ASSEMBLY, 7260A FIGURE 5-1				1		
A1	MAIN PCB ASSEMBLY	475798	89536	475798	1		
A2	FRONT PANEL PCB ASSEMBLY	476028	89536	476028	1		
A3	SIGNAL CONDITIONER	479964	89536	479964	2		1
A4	SIGNAL CONDITIONER	479964	89536	479964	REF		1
A5	TIMEBASE PCB ASSEMBLY	406918	89536	406918	1		
F1	FUSE, SLO-BLO				1	5	
	FUSE, SLO-BLO, 3/8 AMP (100/120V)	109264	71400	MDL3-8			
	FUSE, SLO-BLO, 3/16 AMP (220/240V)	501098	71400	MDL3-16			
H1	GROMMET	104273	72653	7582	1		
H2	LUG, SOLDER	167015	73734	118100	1		
H3	NUT, HEX 4-40	110635	73734	8003NP	2		
H4	NUT, HEX	110916	73734	17-200NP	2		
H5	NUT, SELF-LOCKING	152819	78199	511-061800-00	4		
H6	SCREW, FHP, 6-32 X 5/8	114876	89536	114876	6		
H7	SCREW, PHP, 4-40 X 1/2	152132	73734	19026	2		
H8	SCREW, TAPTITE, 6-32 X 3/8, BLK	485227	89536	485227	6		
H9	SCREW, SEMS, 6-32 X 3/8	177022	89536	177022	2		
H10	SCREW, PHP, 4-40 X 1/2	256172	89536	256172	2		
H11	SCREW, PH THD FORMING, 6-20 X 3/8	288266	89536	288266	1		
H12	WASHER, EXT TOOTH	175943	89536	175943	1		
H13	WASHER, INTERNAL LOCK #4	110403	73734	99402	2		
H14	WASHER, SHOULDER	485417	86928	5607-50	1		
H15	WASHER, SPLIT #4	110395	89536				
J1	CONNECTOR, BCD	152033	95712	30355-1	4		
J2	CONNECTOR, BCD	152033	95712	30355-1	REF		
J3	CONNECTOR, BCD	152033	95712	30355-1	REF		
J4	CONNECTOR, BCD	152033	95712	30355-1	REF		
J5	CONNECTOR, SUB-MINI 3-PIN (ACC POWER)	479410	81312	SM3PN	1		
MP1	BUSHING, INSULATED	488429	89536	488429	1		
MP2	PUSHBUTTON, BLUE	486472	89536	486472	4		
MP3	PUSHBUTTON, LITE GREY	486480	89536	486480	1		
MP4	PUSHBUTTON, GREEN	486498	89536	486498	1		
MP5	BUTTRESS, SUPPORT	481796	89536	481796	1		
MP6	COVER, BOTTOM ASSEMBLY	489302	89536	489302	1		
MP7	COVER, CONNECTOR	488395	89536	488395	1		
MP8	HEAT SINK	473868	89536	473868	1		
MP9	INSULATOR, XSTR	412809	13103	43-03-2	1		
MP10	LABEL, WARNING	386250	89536	386250	1		
MP12	DECAL, FUSE	487330	89536	1			
MP13	PLUG BUTTON	398206	89536	398206	1		
MP14	KNOB ASSEMBLY (CHANNEL A/B AND OFF)	490775	89536	490775	3		
MP16	DECAL, SPECIAL	483073	89536	483073	1		
MP17	COVER, TOP	489310	89536	489310	1		
MP18	LATCH	467548	89536	467548	2		
MP19	NAMEPLATE, SERIAL	472795	89536	472795	1		
S1	SWITCH, TOGGLE SPDT	493825	54659	UL-11	1	1	
T1	TRANSFORMER	486514	89536	486514	1		
U44	IC, LINEAR, VOLTAGE REGULATOR	355107	12040	LM340T-5	1	1	

Table 5-1. Final Assembly (cont)

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
U45	IC, LINEAR, VOLTAGE REGULATOR	413195	12040	LM340T-12	1	1	
U46	IC, LINEAR, VOLTAGE REGULATOR	381665	12040	LM7912T	1	1	
W1	LINE CORD (NOT SHOWN)	343723	89536	343723	1		
W2	WIRE ASSEMBLY, BLACK	504076	89536	504076	1		
W3	WIRE ASSEMBLY, WHITE	504050	89536	504050	1		
W4	WIRE ASSEMBLY, GREEN	504068	89536	504068	1		
XF1	FUSEHOLDER W/NUT	460329	89536	460329	1		
	FUSEHOLDER, CAP	460238	89536	460238	1		
	INSTRUCTION MANUAL (NOT SHOWN)	487504	89536	487504	1		

1 THE RESISTOR HAS BEEN PRESELECTED FOR A3 AND A4 HYBRID SIGNAL CONDITIONER AND MUST BE INSTALLED WITH THE HYBRIDS AS A COMBINATION.

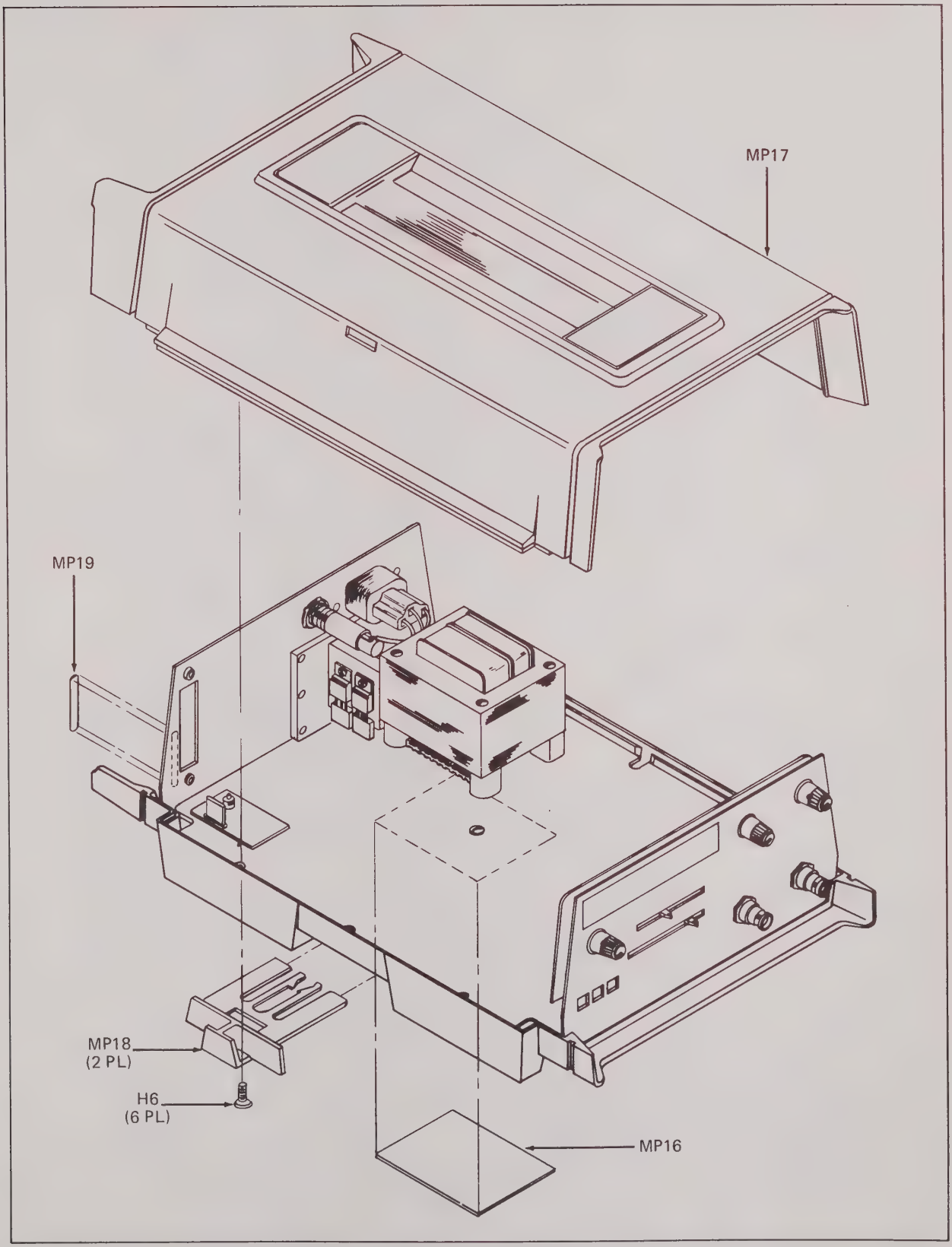

Figure 5-1. Final Assembly

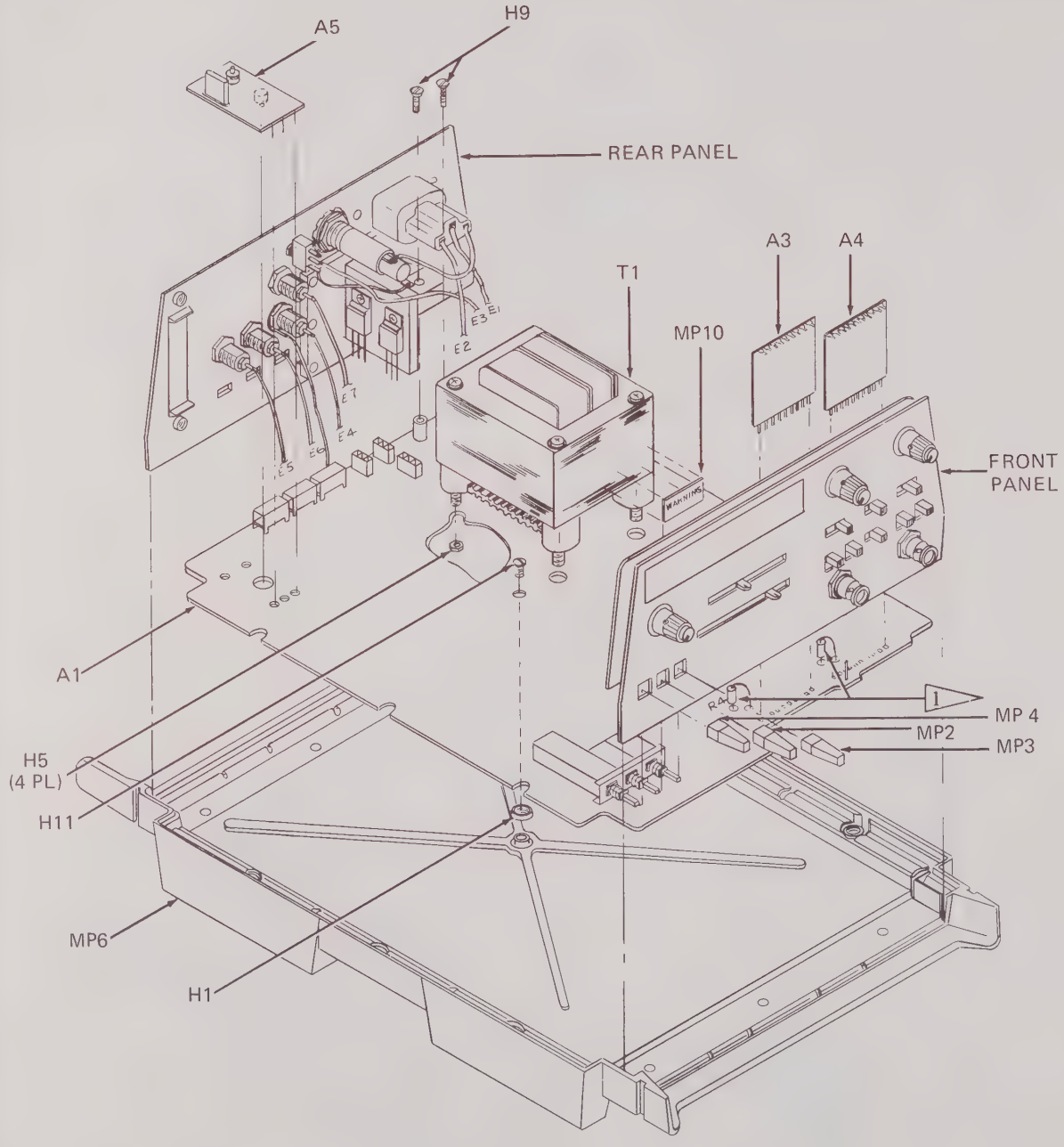

Figure 5-1. Final Assembly (cont)

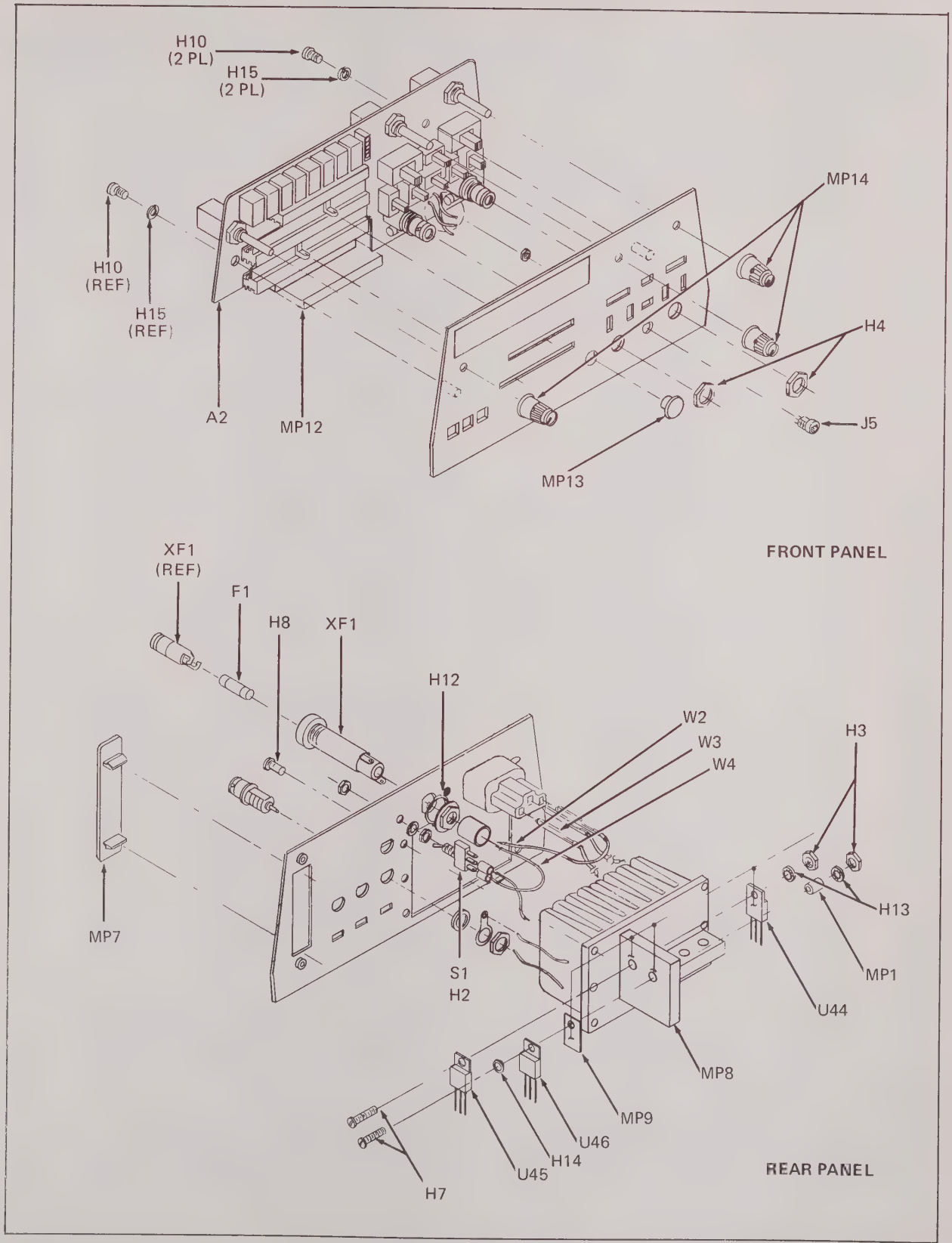

Figure 5-1. Final Assembly (cont)

Table 5-2. A1 Main PCB Assembly

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
A1	Ⓐ MAIN PCB ASSEMBLY	475798	89536	475798	REF		
	FIGURE 5-2 (7260A-4001T)						
C1	CAP, ELECT, 470 UF -10/+75%, 35V	478792	89536	478792	2		
C2	CAP, ELECT, 470 UF -10/+75%, 35V	478792	89536	478792	REF		
C3	CAP, ELECT, 1000 UF -10/+75%, 25V	478826	89536	478826	1		
C4	CAP, ELECT, 6800 UF -10/+100%, 15V	478784	89536	478784	1		
C5	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	5		
C6	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C7	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C8	CAP, CER, 0.0012 UF +/-20%, 100V	106732	71590	CF122	2		
C9	CAP, CER, 0.1 UF +/-GMV, 10V	368647	71490	UK10-104	2		
C10	CAP, CER, 0.025 UF +/-20%, 100V	168435	56289	C023B101H253M	1		
C11	CAP, MICA, 220 PF +/-5%, 500V	170423	72136	DM15F221J	2		
C12	CAP, TA, 1 UF +/-20%, 35V	161919	56289	196D105X0035JA1	1		
C13	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	28		
C14	CAP, CER, 0.1 UF +/-GMV, 10V	368647	71490	UK10-104	REF		
C15	CAP, TA, 39 UF +/-20%, 20V	358234	56289	196D396X0020PE4	1		
C16	CAP, MICA, 5000 PF +/-5%, 500V	181065	72136	DM19F502J	1		
C17	CAP, CER, 0.0012 UF +/-20%, 100V	106732	71590	CF122	REF		
C18	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C19	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C20	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C21	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C22	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C23	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C24	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C25	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C26	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C27	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C28	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C29	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C30	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C31	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C32	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C33	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C34	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C35	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C36	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C37	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C38	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C39	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C40	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C41	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C42	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C43	CAP, MICA, 220 PF +/-5%, 500V	170423	72136	DM15F221J	REF		
C44	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C45	CAP, CER, 3300 PF +/-20%, 100V	106674	56289	C023B102F332M	1		
C46	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C47	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C48	CAP, TA, 330 UF +/-10%, 6V	193011	56289	196D331X0006KA1	1		

Table 5-2. A1 Main PCB Assembly (cont)

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
C49	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
CR3	DIODE, GE, 80 MA, 100 PIV	149187	07933	1N270	2	1	
CR4	DIODE, GE, 80 MA, 100 PIV	149187	07933	1N270	REF		
CR5	DIODE, RECTIFIER BRIDGE, 1.5 AMP	296509	21845	F903C-22	2	1	
CR6	DIODE, RECTIFIER BRIDGE, 1.5 AMP	296509	21845	F903C-22	REF		
CR7	DIODE, RECTIFIER BRIDGE, SI, 2 AMP	347559	05277	1N5400	2	1	
CR8	DIODE, RECTIFIER BRIDGE, SI, 2 AMP	347559	05277	1N5400	REF		
J2	SOCKET, PCB MTG	376418	22526	75060-007	24		
J3	SOCKET, PCB MTG	376418	22526	75060-007	REF		
J6	CONNECTOR, RECEPTACLE	291948	00779	583650-7	1		
JB1	CONNECTOR, AMP PIN	484428	00779	9-87022-1	94		
JB2	CONNECTOR, AMP PIN	484428	00779	9-87022-1	REF		
L1	CHOKE, 6-TURN	320911	89536	320911	1		
MP1	GUIDE, PIN	375840	89536	375840	1		
MP2	KEY, POLARIZING	424572	00779	530286-2	1		
P1	CONNECTOR, AMP PIN	484428	00779	9-87022-1	REF		
P4	CONNECTOR, AMP PIN	484428	00779	9-87022-1	REF		
Q1	XSTR, PNP, HI-SPEED SWITCH (SELECTED)	369629	89536	369629	2	1	
Q2	XSTR, PNP, HI-SPEED SWITCH (SELECTED)	369629	89536	369629	REF		
Q3	XSTR, SI, NPN	218396	04713	2N3904	2	1	
Q4	XSTR, SI, NPN	218396	04713	2N3904	REF		
Q5	XSTR, SI, PNP	195974	04713	2N3906	2	1	
Q7	XSTR, SI, PNP	325753	09214	D45C5	1	1	
Q8	XSTR, SI, PNP	195974	04713	2N3906	REF		
R1	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-4-5P470E	6		
R2	RES, VAR, 10K +/-20%, 0.20W	369553	54869	PT10V-10K	2	1	
R3	RES, SIG. COND, MATCHED TO A4(NOT SHOWN)				1		1
R4	RES, SIG. COND, MATCHED TO A3(NOT SHOWN)				1		1
R5	RES, MTL. FILM, 4.99K +/-1%,, 1/8W	168252	91637	CMF554991F	2		
R6	RES, MTL. FILM, 4.99K +/-1%, 1/8W	168252	91637	CMF554991F	REF		
R7	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-4-5P4K7	4		
R8	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	2		
R9	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-4-5P470E	REF		
R10	RES, COMP, 100 +/-5%, 1/4W	147926	01121	CB1015	1		
R11	RES, DEP. CAR, 150 +/-5%, 1/4W	343442	80031	CR251-4-5P150E	2		
R12	RES, VAR, 10K +/-20%, 0.20W	369553	54869	PT10V-10K	REF		
R13	RES, DEP. CAR, 470K +/-5%, 1/4W	342634	80031	CR251-4-5P470K	1		
R14	RES, DEP. CAR, 1.8K +/-5%, 1/4W	441444	80031	CR251-4-5P1K8	1		
R15	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	REF		
R16	RES, DEP. CAR, 560 +/-5%, 1/4W	385948	80031	CR251-4-5P560E	2		
R17	RES, COMP, 510 +/-5%, 1/4W	218032	01121	CB5115	1		
R18	RES, DEP. CAR, 4.7 +/-5%, 1/4W	342683	80031	CR251-45P4E7	1		
R19	RES, DEP. CAR, 51 +/-5%, 1/4W	414540	80031	CR251-4-5P51E	1		
R20	RES, DEP. CAR, 13K +/-5%, 1/4W	441420	80031	CR251-4-5P13K	2		
R22	RES, COMP, 4.7K +/-5%, 1/4W	148072	01121	CB4725	3		
R23	RES, DEP. CAR, 13K +/-5%, 1/4W	441420	80031	CR251-4-5P13K	REF		
R24	RES, DEP. CAR, 150 +/-5%, 1/4W	343442	80031	CR251-4-5P150E	REF		
R25	RES, COMP, 27 +/-5%, 1/4W	160812	01121	CB2705	1		
R26	RES, COMP, 4.7K +/-5%, 1/4W	148072	01121	CB4725	REF		
R27	RES, DEP. CAR, 560 +/-5%, 1/4W	385948	80031	CR251-4-5P560E	REF		

Table 5-2. A1 Main PCB Assembly (cont)

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
R28	RES, COMP, 4.7K +/-5%, 1/4W	148072	01121	CB4725	REF		
R29	RES, COMP, 4.7K +/-5%, 1/4W	148072	01121	CB4725	REF		
R30	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-45P470E	REF		
R31	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-45P4K7	REF		
R32	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-45P470E	REF		
R33	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-45P470E	REF		
R34	RES, COMP, 470 +/-5%, 1/4W	147983	01121	CB4715	2		
R35	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-45P470E	REF		
R36	RES, COMP, 470 +/-5%, 1/4W	147983	01121	CB4715	REF		
R37	RES, DEP. CAR, 100 +/-5%, 1/4W	348771	80031	CR251-45P100E	1		
R38	RES, COMP, 560 +/-5%, 1/4W	147991	01121	CB5615	4		
R39	RES, COMP, 560 +/-5%, 1/4W	147991	01121	CB5615	REF		
R40	RES, COMP, 68 +/-5%, 1/4W	147918	01121	CB6805	1		
R41	RES, COMP, 180 +/-5%, 1/4W	147942	01121	CB1815	2		
R42	RES, DEP. CAR, 47 +/-5%, 1/4W	441592	80031	CR251-45P47E	2		
R43	RES, DEP. CAR, 1M +/-5%, 1/4W	348987	80031	CR251-45P1M	1		
R44	RES, COMP, 10K +/-5%, 1/4W	148106	01121	CB1035	2		
R45	RES, COMP, 10K +/-5%, 1/4W	148106	01121	CB1035	REF		
R46	RES, DEP. CAR, 47 +/-5%, 1/4W	441592	80031	CR251-45P47E	REF		
R47	RES, DEP. CAR, 20K +/-5%, 1/4W	441477	80031	CR251-45P20K	3		
R48	RES, DEP. CAR, 20K +/-5%, 1/4W	441477	80031	CR251-45P20K	REF		
R49	RES, DEP. CAR, 20K +/-5%, 1/4W	441477	80031	CR251-45P20K	REF		
R50	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251_45P4K7	REF		
R51	RES, DEP. CAR, 22 +/-5%, 1/4W	381145	80031	CR251-45P22E	REF		
R52	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-45P4K7	REF		
R53	RES, COMP, 300 +/-5%, 1/4W	348276	01121	CB3015	1		
R54	RES, COMP, 180 +/-5%, 1/4W	147942	01121	CB1815	REF		
R55	RES, COMP, 560 +/-5%, 1/4W	147991	01121	CB5615	REF		
R56	RES, COMP, 560 +/-5%, 1/4W	147991	01121	CB5615	REF		
R57	RES, COMP, 270 +/-5%, 1/4W	160804	01121	CB2715	1		
R58	RES, COMP, 820 +/-5%, 1/4W	148015	01121	CB8215	1		
R59	RES, DEP. CAR, 1.3 +/-5%, 1/4W	442012	80031	CR251-4-5P1ES	1		
RN1	RESISTOR NETWORK, 39, 14-PIN	412866	89536	412866	1	1	
RN2	RESISTOR NETWORK, 4.7K, DIP	387100	89536	387100	1	1	
RN3	RESISTOR NETWORK, 560, SIP	484451	89536	484451	1	1	
RN4	RESISTOR NETWORK, 4.7K, 6-PIN, SIP	494690	89536	494690	2	1	
RN5	RESISTOR NETWORK, 4.7K, 6-PIN, SIP	494690	89536	494690	REF		
RN6	RESISTOR NETWORK, 4.7K, 8-PIN, SIP	412916	89536	412916	1	1	
S1	PUSHBUTTON ASSY	473991	89536	473991	3		
S2	PUSHBUTTON ASSY	473991	89536	473991	REF		
S3	PUSHBUTTON ASSY	473991	89536	473991	REF		
S4	SWITCH, SLIDE, DPDT	234278	89536	234278	2	1	
S5	SWITCH, SLIDE, DPDT	234278	89536	234278	REF		
S6	SWITCH, SLIDE	354878	89536	354878	3	1	
S7	SWITCH, SLIDE	354878	89536	354878	REF		
S8	SWITCH, SLIDE	354878	89536	354878	REF		
U1	IC, TTL, AND-OR-INVERT GATES T-POLE OUT	412981	01295	SN74LS51N	1	1	
U2	IC, TTL, DECADE DIVIDE X12 BINARY CNTRS	473843	01295	SN74LS92N	1	1	
U3	IC, TTL LO-PWR SCHTKY DUAL J-K FLIP/FLOP	414029	01295	SN74LS112N	1	1	
U4	IC, TTL, SCHTKY, DUAL J-K EDGE-TRIG F/F	363440	01295	SN74S112N	2	1	

Tabel 5-2. A1 Main PCB Assembly (cont)

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
U5	IC, TTL, SCHTKY, DUAL J-K EDGE-TRIG F/F	363440	01295	SN74S112N	REF		
U6	IC, SCHOTTKY, QUAD 2-INPUT	379297	01295	SN74S86N	1	1	
U7	IC, ECL, EDGE-TRIG, J-K FLIP/FLOP	402743	07263	F95029DC	1	1	
U8	IC, DUAL DIFFERENTIAL LINE RECEIVER	404855	01295	SN75115N	1	1	
U9	IC, TTL, HEX INVERTER, POS NAND GATES	393058	01295	SN74LS04N	2	1	
U10	IC, TTL, QUAD, 2-INPUT POS AND GATES	393066	01295	SN74LS08N	2	1	
U11	IC, TTL, QUAD, 2-INPUT, POS NOR GATES	393041	01295	SN74LS02N	1	1	
U12	Ø IC, P-MOS, COUNTER PROGRAM LOGIC	460063	55261	1802	1	1	
U13	Ø IC, MOS, 6-DECADE UP COUNTERS	473215	89536	473215	1	1	
U14	IC, ECL, QUAD, 2-INPUT NOR GATE	504431	07263	F95102	1	1	
U15	IC, OP AMP, GP, EXT. COMPENSATION	352930	89536	352930	1	1	
U16	IC, TTL, QUAD 2-IN, POS/-OR W/TP-OUT	393108	04713	MC74LS32P	2	1	
U17	IC, TTL, QUAD, 2-INPUT POS AND GATES	393066	01295	SN74LS08N	REF		
U18	IC, TTL, LO-PWR SCHTKY DUAL/D CLR/PRESET	393124	01295	SN74LS74N	2	1	
U19	IC, TTL, COUNTER	483594	89536	483594	1	1	
U20	IC, TTL, QUAD, 2-INPUT, POS NAND GATES	393033	01295	SN74LS00N	1	1	
U21	IC, TTL, TRIPLE, 3-INPUT, POS NOR GATES	393090	01295	SN74LS27N	1	1	
U22	IC, TTL LO-PWR SCHTKY TRI-STATE OCT/BUFF	429902	12040	DM81LS95N	2	1	
U23	IC, LINEAR, DUAL TIMER	387407	18324	NE556A	1	1	
U24	IC, TTL, LO-PW SCHTKY DUAL MNSTBL/MLTV	404202	01295	SN74LS221N	2	1	
U25	IC, TTL, TRI, 3-INPUT POS NAND GATES	393074	01295	SN74LS10N	1	1	
U26	IC, TTL, HEX INVERTER, POS NAND GATES	393058	01295	SN74LS04N	REF		
U27	IC, TTL, QUAD 2-IN, POS/-OR W/TP-OUT	393108	04713	MC74LS32P	REF		
U28	IC, TTL, MSI, QUAD, MULTIPLEXER	407833	01295	SN74157N	2	1	
U29	IC, TTL, MSI, QUAD, MULTIPLEXER	407833	01295	SN74157N	REF		
U30	IC, TTL, TRI-STATE QUAD BUFF	355008	12040	DM8093N	1	1	
U31	Ø IC, C-MOS, BCD TO 7-SGMNT LTCH/DCDR/DRVR	429522	04713	MC14511CP	1	1	
U32	IC, TTL, DECADE DIVIDE X 12 BINARY CNTRS	402545	01295	SN74LS90N	1	1	
U33	IC, TTL, LO-PWR SCHTKY DATA SLCTR/MLTPLX	393173	01295	SN74LS151N	1	1	
U34	IC, TTL, LO-PW SCHTKY DUAL MNSTBL/MLTV	404202	01295	SN74LS221N	REF		
U35	IC, TTL, TRI, 3-INPUT POS AND GATES	363457	01295	SN74S11N	1	1	
U36	IC, TTL, DUAL-D, EDG/TRIG F/F	418269	01295	SN74S74N	1	1	
U37	IC, SCHMIT TRIG POS/NAND GATE	483180	01295	SN74S13N	1	1	
U38	IC, PROGRAMMED	454348	89536	454348	1	1	
U39	IC, TTL LO-PWR SCHTKY TRI-STATE OCT/BUFF	429902	12040	DM81LS95N	REF		
U40	Ø IC, MOS TO LED HEX DIGIT DRIVER	429506	12040	DS75492N	2	1	
U41	Ø IC, MOS TO LED HEX DIGIT DRIVER	429506	12040	DS75492N	REF		
U42	IC, TTL, LO-PWR SCHTKY DUAL/D CLR/PRESET	393124	01295	SN74LS74N	REF		
U43	IC, TTL LO-PW SCHTKY 4-1LINE SLCTR/MTPLX	393181	01295	SN74LS153N	1	1	
U45	IC, TTL LO-PWR SCHTKY TRI-STATE OCT/BUFF	429902	12040	DM81LS95N	REF		
U47	IC, TTL, AND/OR E/TP GATES, 2-IN.	495473	01295	SN74S51	1	1	
XU12	SOCKET, IC, 40-PIN	429282	09922	D1LB40P-108	2		
XU13	SOCKET, IC, 40-PIN	429282	09922	D1LB40P-108	REF		
XU44	SOCKET, XSTR, 28-PIN	402958	09922	D1LB-28P-108	3		
XU45	SOCKET, XSTR, 28-PIN	402958	09922	D1LB-28P-108	REF		
XU46	SOCKET, XSTR, 28-PIN	402958	09922	D1LB-28P-108	REF		
XU47							
XU48							

1 SEE PLACEMENT FOR R3 AND R4 RESISTORS ON FIGURE 5-1, MATCHED TO A3 AND A4 SIGNAL CONDITIONERS.

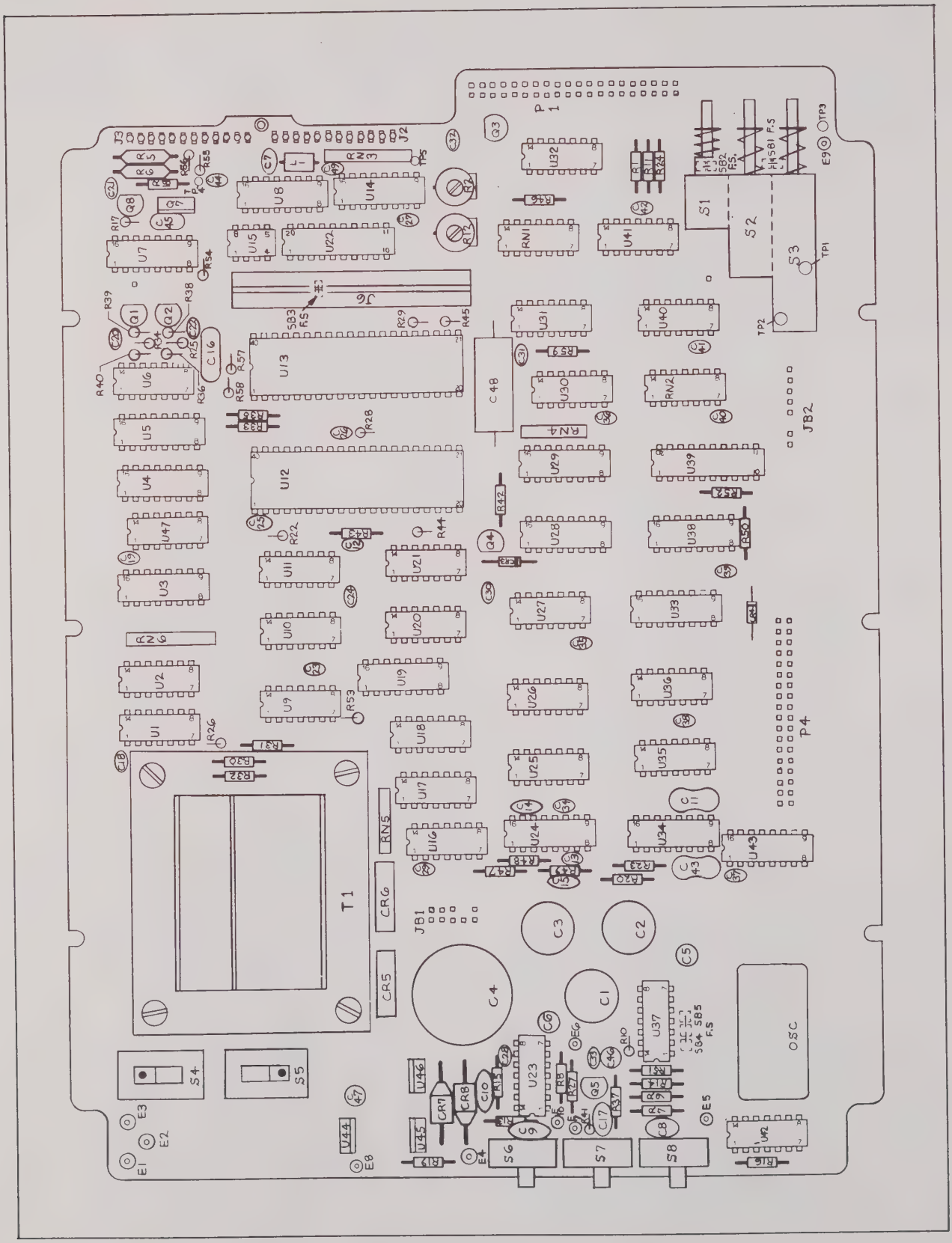

Figure 5-2. A1 Main PCB Assembly

Table 5-3. A2 Front Panel PCB Assembly

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
A2	FRONT PANEL PCB ASSEMBLY FIGURE 5-3 (7261A-4002T)	476028	89536	476028	REF		
C1	CAP, MTL, POLY, 0.68 UF +/-20%, 250V	478651	80031	C281A/AE68K	2		
C2	CAP, MTL, POLY, 0.68 UF +/-20%, 250V	478651	80031	C281A/AE68K	REF		
C3	CAP, TA, 10 UF +/-20%, 15V	193623	56289	196D106X0015KA1	4		
C4	CAP, TA, 10 UF +/-20%, 15V	193623	56289	196D106X0015KA1	REF		
C5	CAP, TA, 10 UF +/-20%, 15V	193623	56289	196D106X0015KA1	REF		
C6	CAP, TA, 10 UF +/-20%, 15V	193623	56289	196D106X0015KA1	REF		
C7	CAP, CER, 33 PF +/-2%, 100V	354852	72982	8121-A100-COG-330G	2		
C8	CAP, CER, 33 PF +/-2%, 100V	354852	72982	8121-A100-COG-330G	REF		
CR1	DIODE, SI HI-SPEED SWITCHING	203323	07910	1N4448	2	1	
CR2	DIODE, SI HI-SPEED SWITCHING	203323	07910	1N4448	REF		
DS1	DISPLAY, LED, RED, 7-SEGMENT	477562	89536	477562	1	1	
DS2	DISPLAY, LED, RED, 7-SEGMENT	477562	89536	477562	REF		
DS3	DISPLAY, LED, RED, 7-SEGMENT	477562	89536	477562	REF		
DS4	DISPLAY, LED, RED, 7-SEGMENT	477562	89536	477562	REF		
DS5	DISPLAY, LED, RED, 7-SEGMENT	477562	89536	477562	REF		
DS6	DISPLAY, LED, RED, 7-SEGMENT	477562	89536	477562	REF		
DS7	DISPLAY, LED, RED, 7-SEGMENT	477562	89536	477562	REF		
DS8	DISPLAY, LED, RED, 7-SEGMENT	477562	89536	477562	REF		
DS9	DISPLAY, LED ARRAY STRIP	483420	28480	HLMP6203	1	1	
DS10	DISPLAY, LED ARRAY STRIP	483412	28480	HLMP6205	1	1	
DS11	DISPLAY, LED ARRAY STRIP	483412	28480	HLMP6205	REF		
DS12	DISPLAY, LED ARRAY STRIP	483412	28480	HLMP6205	REF		
DS13	DISPLAY, LED ARRAY STRIP	483412	28480	HLMP6205	REF		
DS14	DISPLAY, LED ARRAY STRIP	483412	28480	HLMP6205	REF		
DS15	DISPLAY, LED ARRAY STRIP	483420	28480	HLMP6203	REF		
DS16	DISPLAY, LED ARRAY STRIP	483420	28480	HLMP6203	REF		
DS17	DISPLAY, LED, RED	369777	28480	5082-4480	4	1	
DS18	DISPLAY, LED, RED	369777	28480	5082-4480	REF		
DS20	DISPLAY, LED, RED	369777	28480	5082-4480	REF		
DS21	DISPLAY, LED, RED	369777	28480	5082-4480	REF		
F2	FUSE, FAST ACTING	494930	75915	212.250	2	10	
F3	FUSE, FAST ACTING	494930	75915	212.250	REF		
H1	SCREW, PH, THD-FORMING, 2-28 X 13/32	493957	89536	493957	9		
H2	SPACER, LED	426882	89536	426882	3		
J1	CONNECTOR, 40-PIN	460030	00779	5182-383-4	1		
J9	CONNECTOR, BCN, CHANNEL A	479162	55331	1067-000-801	2		
	SOCKET, IN-LINE, 10-PIN	477661	00779	583773-3	2		
J10	CONNECTOR, BCN, CHANNEL B	479162	55331	1067-000-801	REF		
	SOCKET, IN-LINE, 10-PIN	477661	00779	583773-3	REF		
J11	CONNECTOR, HORIZONTAL JACK, BLACK	149112	74970	105-0753	1		
MP1	CARRIER, 10-POS	477851	00779	435999-2	1		
MP2	CARRIER, 10-POS	477851	00779	435999-2	REF		
MP3	CARRIER, 7-POS	477737	00779	435999-1	1		
MP4	DETENT SPRING	472878	00779	435996	2		
MP5	WIPER GUIDE	472886	00779	435998	2		
MP6	SPACER, LED (DS9 THRU DS15)	426882	89536	426882	3		
R1	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	3		
R2	RES, MTL. FILM, 402K +/-1%, 1/8W	217984	91637	CMF554023F	4		

Table 5-3. A2 Front Panel PCB Assembly (cont)

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
R3	RES, MTL. FILM, 402K +/-1%, 1/8W	217984	91637	CMF554023F	REF		
R4	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	REF		
R5	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	REF		
R6	RES, COMP, 2K +/-5%, 1/2W	169854	01121	EB2025	4		
R7	RES, COMP, 2K +/-5%, 1/2W	169854	01121	EB2025	REF		
R8	RES, MTL. FILM, 402K +/-1%, 1/8W	217984	91637	CMF554023F	REF		
R9	RES, COMP, 2K +/-5%, 1/2W	169854	01121	EB2025	REF		
R10	RES, COMP, 2K +/-5%, 1/2W	169854	01121	EB2025	REF		
R11	RES, MTL. FILM, 402K +/-1%, 1/8W	217984	91637	CMF554023F	REF		
R12/S13	RES, VAR, CER, W/S, 1M +/-10%, 1/2W	478966	89536	478966	1	1	
R13/S9	RES, VAR, CER, W/S, 5K +/-10%, 1/2W	478974	89536	478974	2	1	
R14/S10	RES, VAR, CER, W/S, 5K +/-10%, 1/2W	478974	89536	478974	REF		
R15	RES, DEP. CAR, 25 +/-5%, 1/4W	442210	80031	CR251-4-5P25E	2		
R16	RES, DEP. CAR, 25 +/-5%, 1/4W	442210	80031	CR251-4-5P25E	REF		
S1	SWITCH, SLIDE, ACTIVATOR	454371	00779	435995	2	1	
S2	SWITCH, SLIDE, ACTIVATOR	454371	00779	435995	REF		
S3	SWITCH, SLIDE, 3-POS	453183	89536	453183	2	1	
S4	SWITCH, SLIDE, SPDT	429332	09353	1101-M2-C-Q	6	2	
S5	SWITCH, SLIDE, 3-POS	453183	89536	453183	REF		
S6	SWITCH, SLIDE, SPDT	429332	09353	1101-M2-C-Q	REF		
S7	SWITCH, SLIDE, SPDT	429332	09353	1101-M2-C-Q	REF		
S8	SWITCH, SLIDE, SPDT	429332	09353	1101-M2-C-Q	REF		
S9/R13	RES, VAR, CER, W/S, 5K +/-10%, 1/2W	478974	89536	478974	REF		
S10/R14	RES, VAR, CER, W/S, 5K +/-10%, 1/2W	478974	89536	478974	REF		
S11	SWITCH, SLIDE, SPDT	429332	09353	1101-M2-C-Q	REF		
S12	SWITCH, SLIDE, SPDT	429332	09353	1101-M2-C-Q	REF		
S13/R12	RES, VAR, CER, W/S, 1M +/-10%, 1/2W	478966	89536	478966	REF		
U1	IC, LINEAR, OP AMP	473777	89536	473777	1	1	

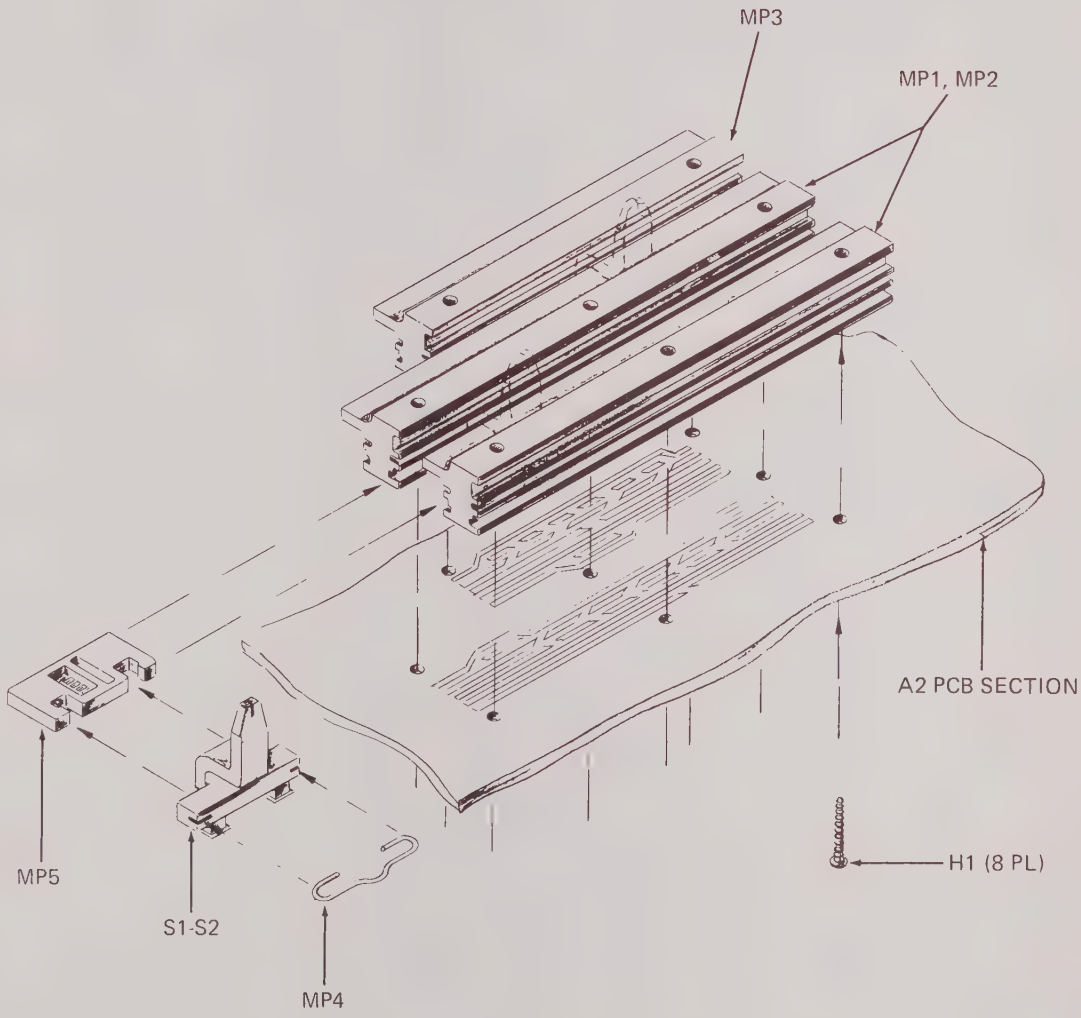

Figure 5-3. A2 Front Panel PCB Assembly

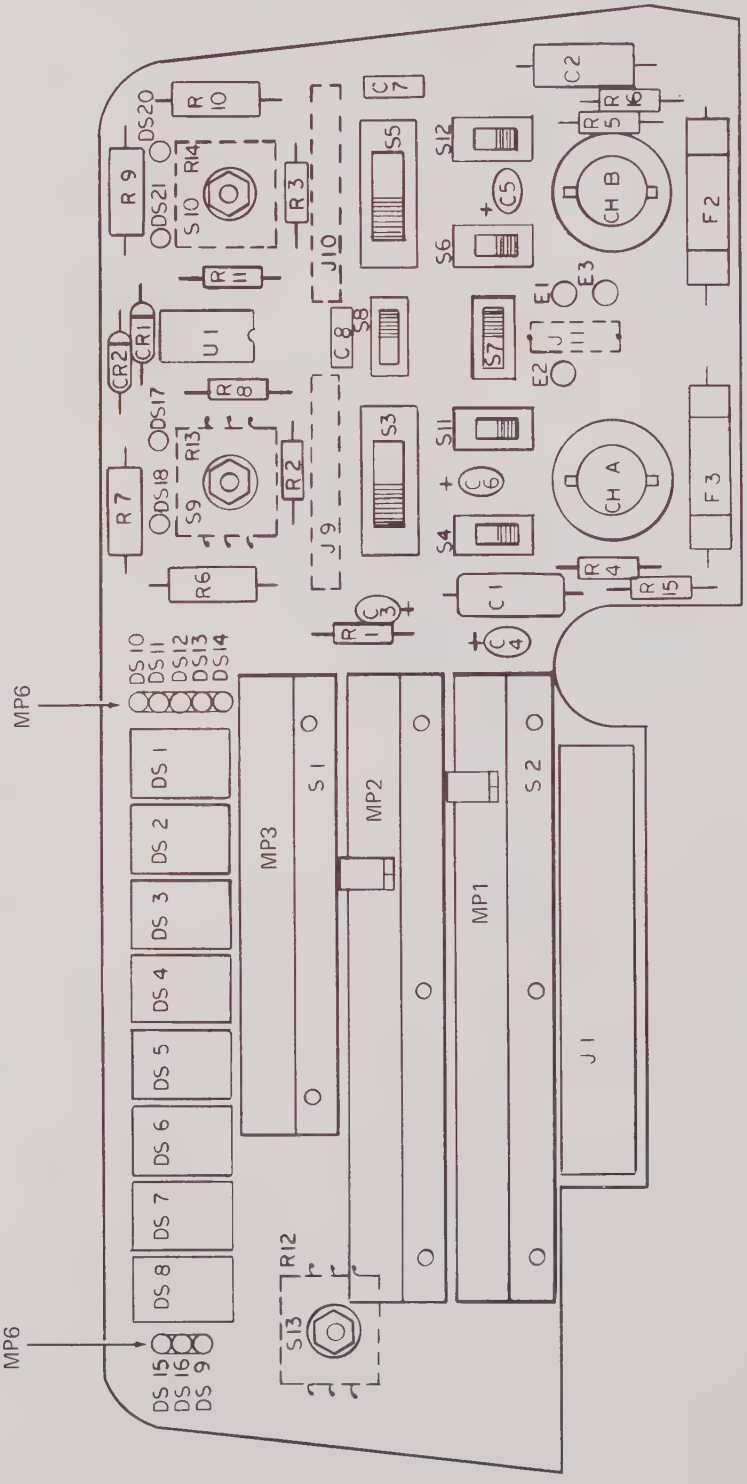

Figure 5-3. A2 Front Panel PCB Assembly (cont)

Table 5-4. A5 Time Base PCB Assembly

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
A5	TIMEBASE PCB ASSEMBLY FIGURE 5-4 (1952B-4010T)	406918	89536	406918	REF		
C1	CAP, VAR, 22 PF, 100V	369207	80031	C010KA/20E	2		
C2	CAP, VAR, 22 PF, 100V	369207	80031	C010KA/20E	REF		
C3	CAP, CER, 22 PF +/-20%, 1000V	369157	56289	C030B102F220M	2		
C4	CAP, CER, 22 PF +/-20%, 1000V	369157	56289	C030B102F220M	REF		
C5	CAP, CER, .01 UF +/-5%, 16V	368639	14655	HCC16103P	1		
L1	CHOKE, 6-TURN	320911	89536	320911	1		
MP1	PINS, CONTACT	376574	00779	3-87022-1	5		
Q1	XSTR, N-CHANNEL, SILICON JUNCTION	386094	01295	A5T3819/SX3819	2		
Q2	XSTR, N-CHANNEL, SILICON JUNCTION	386094	01295	A5T3819/SX3819	REF		
R1	RES, COMP, 1M +/-10%, 1/8W	435008	01121	BB1051	1		
R2	RES, COMP, 1K +/-10%, 1/8W	153916	01121	BB1021	3		
R3	RES, COMP, 1K +/-10%, 1/8W	153916	01121	BB1021	REF		
R4	RES, COMP, 1K +/-10%, 1/8W	153916	01121	BB1021	REF		
Y1	CRYSTAL, QUARTZ	385732	89536	385732	1		

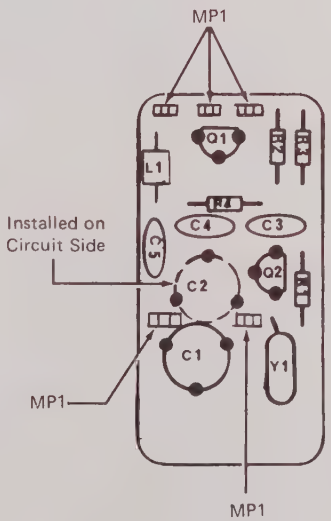

Figure 5-4. A5 Time Base PCB Assembly

Section 6
Option & Accessory Information

TABLE OF CONTENTS

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	ACCESSORIES	600-1
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72XXA-010	Battery Pack	010-1
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72XXA-131	Low Power Oven Time Base	131-1
72XXA-132	Superior Low Power Oven Time Base	132-1
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72XXA-331	1300 MHz Prescaler	6331-1
72XXA-521	Digital Interface PCB Assembly	521-1
72XXA-522 / 72XXA-529	See 72XXA-522/-529 Instrucution Manual	

6-1. INTRODUCTION

6-2. This section of the manual contains information pertaining to the options and accessories available for the 7260A. Where applicable, these descriptions will cover the same range of information as provided in Sections 1-5 of this manual (specifications, installation, theory of operation, etc.). Schematic diagrams for any appropriate option or accessory will be found in Section 3.

6-3. Accessory information can be identified with "600-" paragraph numbers. For options, relevant paragraphs will contain the option number preceded by "6".

Accessories

600-1. GENERAL

600-2. The Table of Contents contains a list of accessories available for use with the 7260A Universal Counter-Timer. The following paragraphs contains descriptions for each type of accessory. Use the accessory model number when ordering.

600-3. Mounting Kits

600-4. Mounting kits suited for the C-size case used with the 7260A are available for standard 19-inch rack or panel format. Each kit comes complete with all mounting hardware. Model Y2014A provides for mounting a single case (size "C") in a 19-inch rack. Model Y2015 mounts two cases ("C") in a 19-inch rack. Model Y2020 mounts a single "C" case in a panel arrangement.

600-5. Instrument Cables

600-6. Two instrument ribbon cables are available for connecting the Data I/O Unit (Option -521) to the Interface PCB Assembly (Option -522), mounted in the 1120A IEEE-488 Translator. The cables, while identical in function, are available in lengths of two feet (Y7203) or five feet (Y7204). The Y7203 cable is supplied with Options -521 or -529 and Option Kits -521K or -529K.

600-7. Filter/Attenuator

600-8. The Model Y7201, as shown in Figure 600-1 is a combination variable attenuator and selectable low-pass filter intended for use as an input signal noise suppressor for Fluke counters. It features a continuously variable X5 to X100 attenuator and a set of three switch-selectable frequency filters; DC to 1 kHz, DC to 20 kHz, or DC to 100 kHz. The Y7201 allows a maximum input signal of 230V ac at 50 Hz for 30 seconds. A BNC connector is provided for convenient attachment to the counter input, and a set of 0.75" spaced banana jacks serve as the input signal connections.

600-9. In operation, the Y7201 attenuates and/or filters unwanted noise/transients from the input signal. These capabilities isolate the counter from the noise levels and, thereby, lessen the possibility of measurement errors.

600-10. To operate the Y7201, use the following procedure:

1. Connect the Y7201 to the CHANNEL A (or CHANNEL B) input to the counter.

2. Select the filter position with the lowest 3 dB point (1 kHz, 20 kHz or 100 kHz) that will accomodate the signal being measured.

3. Turn the ATTEN control fully clockwise (for maximum attenuation).

4. Connect the signal to be measured to the Y7201's banana jacks.

5. Decrease attenuation until a stable display is seen on the counter.

NOTE

For signals that are particularly noisy (or greater than 100V p-p), it may be necessary to add more attenuation and filtering. This operation can be accomplished by adding another Y7201 in series or by adjusting the counter's attenuation and filter controls.

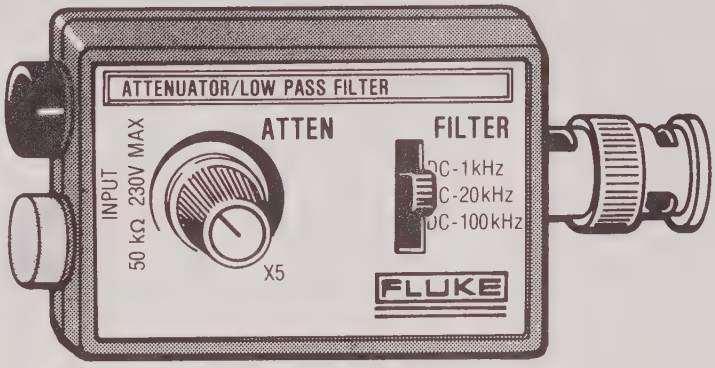


Figure 600-1. Y7201 Filter/Attenuator

Option -010
Battery Pack

010-1. INTRODUCTION

010-2. Option -010 is a nickel-cadmium rechargeable battery unit. The option uses "F" cell nicad batteries for a total capacity of 5.6 amp hours. With a completely discharged battery, charge time is a minimum of 16 hours at room temperature. A discharge cut-off relay has been incorporated to guard against discharging the nicads to too low a level. A thermistor sensor circuit monitors battery temperature and halts the charging if the battery gets too hot. The battery output is fused to protect it against short circuits. Housed in a separate plastic box to eliminate acid corrosion problems, the battery assembly is attached inside the top cover. This option can be installed in the field. Order kit number 72XXA-010K.

010-3. SPECIFICATIONS

010-4. Specifications for the -010 Battery Option are listed in Table 010-1.

010-5. INSTALLATION

010-6. Use the following procedure to install the -010 Battery Option. Refer to Figure 010-1 for installation instructions. Component location can also be determined using Figures 010-3 and 010-4.

1. Remove line power from the instrument.

2. Remove the top cover using the procedure described in Section 4.

3. Place the battery assembly so that the battery and Battery Option PCB are closer to the front of the instrument and the two instrument handle hold-down bolts are through the corresponding holes on the battery bracket.

4. Place the two nuts on the instrument handle hold-down bolts and tighten.

5. Remove the bottom cover using the procedure described in Section 4. Do not remove the Front or Rear Panel assemblies from the Main PCB.

6. Locate solder bridge SB1 near the BTRY/LINE switch on the bottom of the Main PCB. (For 7220A, SB1 is on the front left corner of the bottom of the main PCB). Remove the short. In addition, remove the short on SB6 for the 7261A only.

7. Install the bottom cover.

8. Plug the two cables from the Battery Option PCB into their appropriate connectors on the Main PCB. Grey plug to JB1, black plug to JB2.

9. Fasten the grey ribbon cable under the grey retaining clip (located on the bottom side of the instrument's top cover).

10. Install the top cover of the instrument.

Table 010-1. Specifications

Capacity	5.6 Ampere hours
Battery Type	Four size "F" nicad cells
Charge Time	16 hours minimum at room temperature
Charge Protection	Thermistor actuated shut down of charging circuit if battery gets near 65°C
Discharge Protection	Low voltage automatic shut down at about +4V to prevent battery discharging to a reversed cell condition.

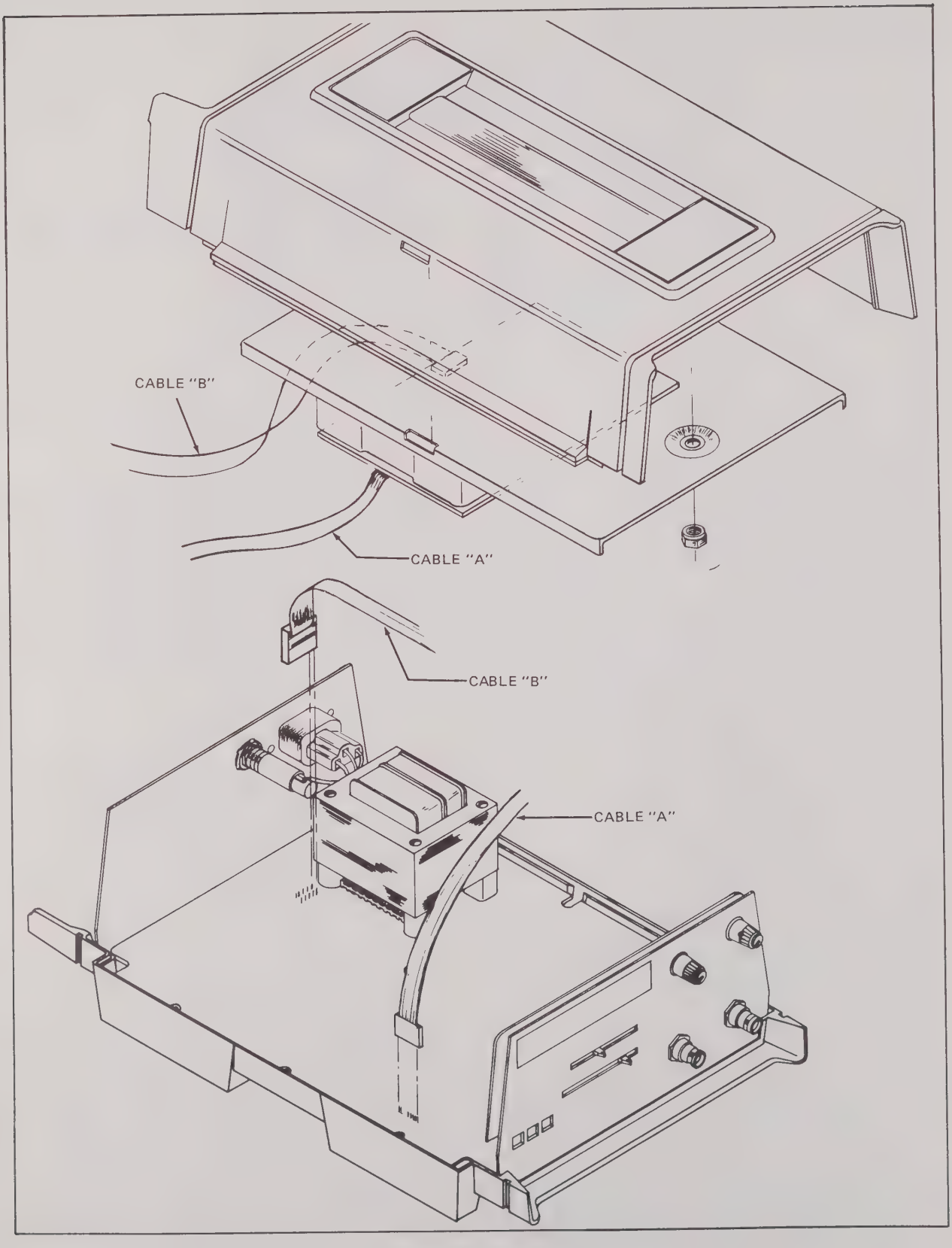


Figure 010-1. Installation

010-7. OPERATION

010-8. To use the battery for instrument power, set the BTRY/LINE switch to the BTRY position. The ON/STBY switch functions normally. The instrument may be powered from the battery with the line cord plugged into line power. This serves no useful purpose, however, and discharges the battery needlessly. When the battery has discharged to about 4V, the low battery voltage relay will remove the instrument load from the battery output, preventing the battery from discharging to too low a level. Place the two POWER switches in the STBY and LINE positions to recharge the battery. After the battery has been charged sufficiently, the RESET switch on the instrument front panel must be pressed to unlatch the low voltage relay and restore normal battery operation.

010-9. If neither oven time base option is installed, the battery will recharge any time the instrument is connected to line power and the power control is set to STBY. The charge rate is maximum when the ON/STBY switch is in the STBY position, and the BTRY/LINE switch is in the LINE position. If the battery is discharged completely, this charge rate will recharge the battery in 16 hours at temperatures around 22°C (72°F). If either oven time base is installed, the BTRY/LINE switch determines which source will power the oven. For maximum charge, the switch must be in the LINE position and the ON/STBY switch must be in the STBY position. If the BTRY/LINE switch is in the BTRY position and the ON/STBY switch is in the STBY position, the oven will draw about 200 mA of the 560 mA charging current. Under these conditions, the battery may not charge completely. If the POWER switches are in the ON and LINE positions, the charging rate will be reduced to prevent overheating inside the instrument. This charge rate is insufficient to recharge the battery but will maintain a float charge on the battery. The thermocouple sensor will halt the charge to keep the battery temperature from exceeding 65°C (149°F). (This will only occur in high ambient temperature environments.) The battery charge will automatically resume when the battery has cooled enough.

NOTE

Battery manufacturers recommend that nicad batteries should not be stored for extended periods of time without recharging at least every 90 days. Storage temperature below 25° C (77° F) is recommended.

010-10. THEORY OF OPERATION

010-11. The theory of operation for the -010 Option will be divided into a basic functional description of the major circuits of the option and a detailed circuit analysis of each circuit.

010-12. BASIC FUNCTIONAL DESCRIPTION

010-13. As Figure 010-2 shows, there are four main sections to the Battery Option PCB circuitry. The Current Source uses +5V unregulated power from the Main PCB to provide the charging current for the battery. The charging rate (high or low) is determined by the position of the ON/STBY switch. The Battery Hi-Temp Circuit reduces the charging current if the battery temperature approaches 65°C. The Low Battery Voltage Relay circuit normally passes the battery power on to the BTRY/LINE switch. Should the battery voltage drop to around 4V, the relay contacts will open, removing the load from the battery. The RESET switch on the instrument front panel must be pressed to restore the Low Battery Voltage Relay Circuit. If the BTRY/LINE switch is in the BTRY position, the +5V power from the battery is connected to the ON/STBY switch, and the oven if an oven time base is installed. If the ON/STBY switch is in the ON position, the battery power is supplied to the instrument and the Inverter circuit. The Inverter circuit provides operating voltages for the -5V, +12V and -12V regulators.

010-14. DETAILED CIRCUIT ANALYSIS

010-15. The Battery Option Schematic in Section 8 will be used to illustrate the detailed circuit analysis. The battery and thermistor are located inside the battery case.

010-16. Battery Hi-Temp Circuit

010-17. The Battery Hi-Temp Circuit is an inverting amplifier that protects the battery by reducing the battery charging current as the battery temperature approaches 65°C. It does this by altering the bias voltage of the Current Source controller to turn off the current source. The inverting amplifier is U1B with thermistor RT1 used as the feedback resistor. The positive input of the op amp is COMMON. The negative input is the -12V coupled through R9. RT1 is located next to the battery. When the battery is about 22°C, the resistance of RT1 will be about 50Ω. At this time, the output of the inverting amplifier (felt at the lower junction of R7 and R8) is about +.4V. RT1 exhibits a positive temperature coefficient. As the battery temperature rises, the resistance of RT1 increases. When the battery temperature approaches 65°C, the resistance of RT1 passes over a sharp knee and approaches 500Ω. The output of the negative gain amplifier approaches +5V.

010-18. Current Source

010-19. The Current Source uses the unregulated +5V from the Main PCB to provide charging current for the

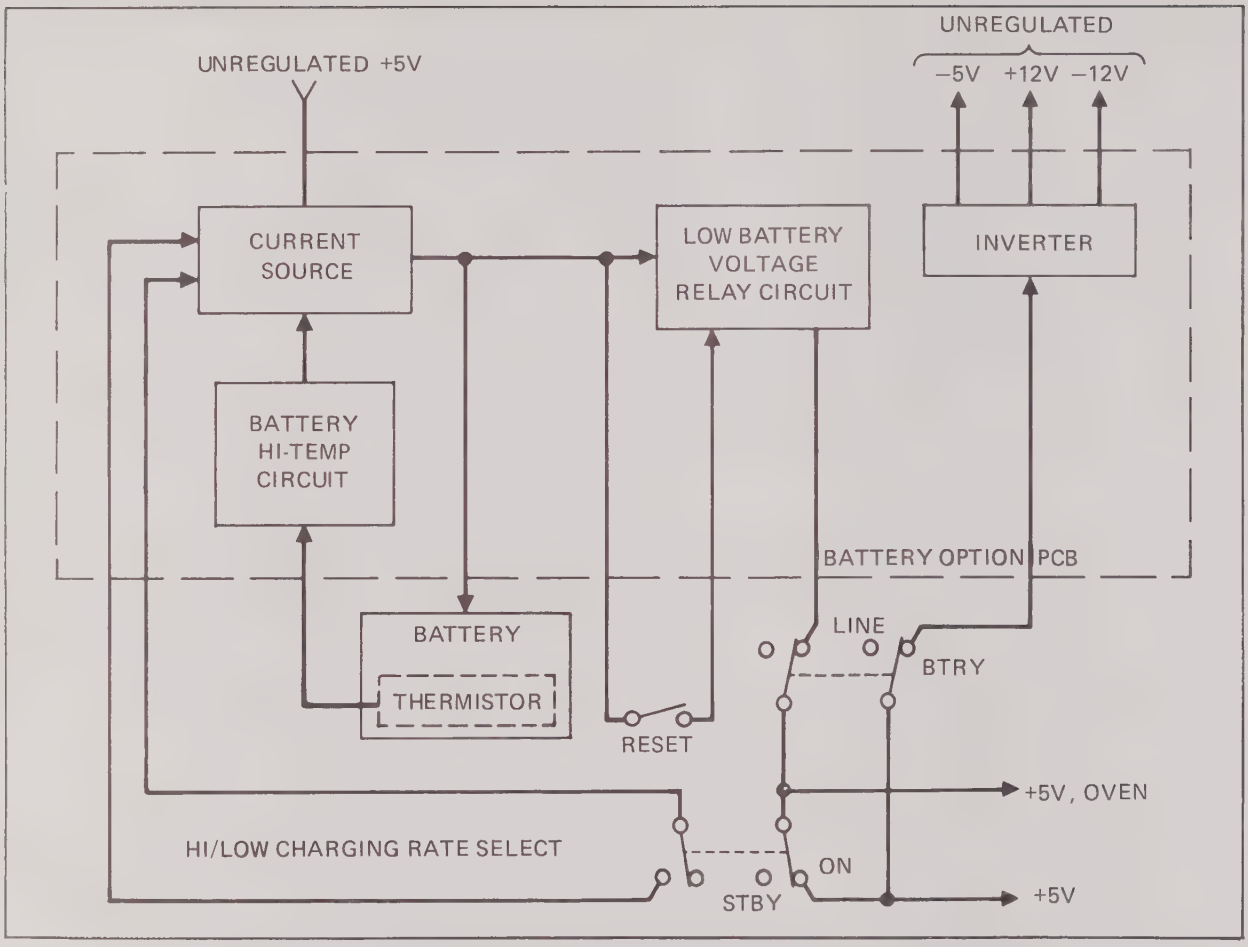


Figure 010-2. -010 Option Block Diagram

battery. This circuit consists of the series pass element, Q1; the sensing element, R1; the control element, U1A; and their associated circuitry. Q1 directly controls the current charging the battery. The base bias of Q1 is in turn controlled by the output of U1A. The positive input is battery voltage felt on the battery side of R1 (TP2). The negative input is picked off the voltage divider network composed of R2, R8 and sometimes R7. The voltage divider is between the input side of R1 (TP1) and the output of the Battery Hi-Temp circuit.

010-20. The charging current is changed by altering the input to U1A from the voltage divider. The voltage divided input is altered by changing the position of the ON/STBY switch. When the switch is in the STBY position, R7 is placed in parallel with R8. Their combined resistance is about one-fifth that of R8 alone. At normal operating temperatures, the bottom of the voltage divider is at +0.5V and the top is at battery voltage plus the voltage drop across R1. The op amp causes Q1 to pass nominally 560 mA through R1. If the ON/STBY switch is in the ON position, R7 is no longer in parallel with R8. This change in the voltage divider input to U1A will cause the charging current to decrease to nominally 110 mA. If the battery temperature approaches 65° C, the bottom of the voltage divider becomes +5V and the voltage at TP1 approaches the battery voltage. This decreases the output of the op amp cutting off Q1. As the battery cools, the resistance of the thermistor decreases allowing the battery charge to resume. If F1 blows, removing the regulated input to U1A, CR10 will limit the conduction of Q1 so that the voltage at TP2 does not exceed 6V.

010-21. Low Battery Voltage Relay Circuit

010-22. The low battery voltage relay keeps the battery from discharging to a reversed cell condition by removing the battery load when battery voltage drops to about 4V. The battery is connected to its load through K1, a two coil latching relay. During normal operation, the battery and its load are connected, Q2 and Q6 are off and Q5 is in saturation. When battery voltage drops to about 4V, the base bias on Q5 (TP5) is low enough to cut Q5 off. This lets the input on pin 13 of flip-flop U2 rise. This will

change the state of U2 making the output on pin 11 of U2 go low. This causes Q6 to conduct, charging C2 and turning Q2 on. When Q2 conducts, the coil of K1 in the collector of Q2 will energize, opening K1. When K1 removes the battery loads, the input circuitry for Q2 is deenergized. C2 has been charged to make Q2 conduct long enough to insure that K1 is latched in the open condition. After the battery has been recharged, pressing the RESET switch on the front panel will connect battery voltage to both the reset coil of K1 and pin 6 of U2. The RESET switch contacts will be closed long enough to insure that K1 will be latched shut. This will restore the connection between the battery and its load. Q5 will go into saturation. The battery voltage at pin 6 of U2 will cause pin 11 to go high, turning off Q6.

010-23. Inverter

010-24. The Inverter is composed of Q3, Q4, T1 and their associated circuitry. The three components form an oscillator that runs at about 10 kHz. This oscillation allows T1 to step up the battery voltage to provide rectified operating voltages to the -5V, +12V and -12V regulators for instrument power.

010-25. PERFORMANCE TEST

010-26. Use the following procedure as a performance test. Table 010-2 lists the test points. The component location diagram at the end of this option can be used to locate these test points. The instrument will be referred to as the UUT (Unit Under Test). Use a variable DC power supply with an output range of at least 3-5V and the test equipment listed in Section 4.

1. Remove the top cover of the UUT using the procedure given in Section 4. Leave the cables from the Battery Option PCB connected to the Main PCB and lay the top cover beside the instrument, upside-down. The grey ribbon cable will have to be removed from the retaining clip on the bottom side of the top cover.

Table 010-2. Test Points

TEST POINTS	COMMENTS
TP1, TP2	Voltage across sensing resistor, R1.
TP3	COMMON
TP4	Battery voltage.
TP5	Low Battery Voltage Sensing Point
TP6	Low Battery Voltage Cut-Off Signal.

2. Connect the UUT to line power.

3. On the UUT front panel:

   a. Set the ON/STBY switch to the STBY position.

   b. Set the BTRY/LINE switch to the LINE position.

4. Connect the DVM: + to TP2, - to TP3.

5. Verify that the DVM reads greater than 5V. If it does not, continue the charge until this reading (Battery Voltage) is at least 5V.

NOTE

In the next step, the DVM test leads must be isolated from ground.

6. Connect the DVM: + to TP1, - to TP2.

7. Verify that the DVM reads between 96 mV and 128 mV.

8. Set the ON/STBY switch to ON.

9. Verify that the DVM reads between 14 mV and 30 mV.

10. Set the ON/STBY switch to STBY.

11. Connect the DVM: + to TP4, - to TP3.

12. Verify that the DVM reads battery voltage. If there is no voltage present, press the RESET switch on the front panel. The DVM should now read battery voltage.

CAUTION

The counter must be disconnected from ground during the following soldering procedures. Disconnect the power cord and any other connection (e.g., BNC) that may be introducing a ground to the instrument. The use of an ungrounded soldering iron is recommended.

13. Unsolder an end of the fuse wire located on the PCB near the battery harness.

14. Adjust the DC Power Supply for a +5V output.

15. Connect the DC Power Supply + to TP2, - to TP3.

16. Connect the DVM + lead to TP4, – lead to ground.

17. Slowly reduce the DC Power Supply voltage until the relay opens as indicated by the voltage of TP4 dropping suddenly to 0V. (The click of the relay may also be heard.)

18. Verify that the output voltage of the DC Power Supply is between +3.8V and +4.3V.

19. Disconnect the DC Power Supply. Resolder the fuse wire.

20. On the front panel of the UUT:

a. Press and release the RESET switch.

b. Set the ON/STBY switch to the ON position.

c. Set BTRY/LINE switch to the BTRY position.

d. Set the RESOLUTION switch to the 1 kHz position. (For 7220A, 100 Hz.)

e. Set the function select switch to the CHK position.

21. Verify that the UUT display reads 10.000. (For 7220A, display should read 10.0000.)

010-27. MAINTENANCE

010-28. Battery Replacement

010-29. Use the following procedure to replace the battery:

1. Remove the line power from the instrument.

2. Remove the top cover of the instrument using the procedure given in Section 4. Place the top cover upside-down on the work surface.

3. Disconnect the two cables between the Battery PCB and the Main PCB.

4. Remove the four screws holding the battery case to the battery bracket.

5. Note the position of the thermistor. This will be important in a later step.

6. Lift the battery case and Battery Option PCB off the battery and place it to one side.

7. Unsolder the two wires connected to the battery (white and black).

8. Dispose of the old battery.

9. Solder the white and black wires to the tabs on the new battery. White to the tab on the recessed battery end (+) and black to the tab on the flush battery end (–).

10. Replace the battery case being sure to place the thermistor in the same position noted in step 5.

11. Connect the two cables between the Battery PCB and the Main PCB.

12. Replace the top cover.

010-30. Fuse Replacement

010-31. Use the following procedure to replace the fuse on the Battery Option PCB:

1. Remove the line power from the instrument.

2. Remove the top cover from the instrument using the procedure given in Section 4. Place the top cover upside-down on the work surface.

3. Unsolder the ends of F1 from its terminals.

4. Solder a suitable length of #35 magnet wire between the fuse terminals.

5. Place the top cover on the instrument.

010-32. LIST OF REPLACEABLE PARTS

010-33. Table 010-3 is a list of replaceable parts for the battery assembly. Figure 010-3 is the component location diagram for this table.

Table 010-3. Battery Option -010 Assembly

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	NOTE
	⊗ BATTERY OPTION-010 ASSEMBLY FIGURE 6010-3 (7220A-4010T)	OPTION	-010		1		
	BATTERY PCB ASSY	ORDER	BY	OPTION -010	REF		
BT1	BATTERY ASSY	484048	89536	484048	1		
C1	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	6		
C2	CAP, TA, 4.7 UF +/-20%, 25V	161943	56289	196D475X0025KA1	1		
C3	CAP, TA, 330 UF, +/-10%, 6V	193011	56289	150D337X9006S	1		
C4	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C5	CAP, CER, 47 PF +/-20%, 1000V	369132	56289	C030B102H470J	1		
C6	CAP, CER, 0.1 UF +/-GVM, 25V	369199	71590	UK-25-104	1		
C7	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C8	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C9	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C10	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
CR1	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	9	2	
CR2	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR3	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR4	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR5	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR6	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR7	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR8	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR9	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR10	DIODE, ZENER, 7.5V	256446	07910	1N755B	1		
H1	NUT, HEX, #4	147611	89536	147611	2		
H2	SCREW, PHP, 4-40 X 1/4	129890	73734	19022	1		
H3	SCREW, PHP, 6-32 X 1/4	152140	73734	19042	8		
H4	SCREW, RHD, PH, 4-40 X 3/8	152124	73734	18024	2		
H5	SPACER	500074	89536	500074	4		
H6	WASHER, FLAT #8	110288	73734	97425	4		
H7	WASHER, FIBER	246488	73734	1471	4		
H8	WASHER, #6	110338	89536	110338	8		
H9	WASHER, #6	152140	89536	152140	4		
H10	WASHER, LOCK #4	110403	73734	1302	2		
H11	WASHER, SHOULDER, INSULATING	485417	86928	5607-50	1		
H12	WASHER, SPLIT #4	110395	89536	110395	1		
K1	RELAY, LATCHING	484535	89536	484535	1		
L1	CHOKE	502138	89536	502138	1		
MP1	BRACKET, BATTERY	476200	89536	476200	1		
MP2	CASE, BATTERY	475459	89536	475459	1		
MP3	CABLE TIE	172080	06383	SST-1M	1		
MP4	INSULATOR, REG.	412809	13103	43-77-8	1		
MP5	PLUG, CONNECTOR KEY (NOT SHOWN)	500801	52152	3435-0000	1		
MP6	SPACER, PCB COMPONENT (NOT SHOWN)	296319	89536	296319	1		
MP7	SPACER, XSTR (TO Q2) (NOT SHOWN)	152207	07047	10123-DAP	1		
Q1	TRANSISTOR, SI, NPN, PWR	325761	09214	D44C5	1	1	
Q2	XSTR, SI, NPN	346916	89536	346916	1	1	
Q3	XSTR, SI, NPN, PWR	325720	04713	MJE3055	2	1	
Q4	XSTR, SI, NPN, PWR	325720	04713	MJE3055	REF		

Table 010-3. Battery Option -010 Assembly (cont)

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	NOTE
Q5	XSTR, SI, NPN	218396	04713	2N3904	1	1	
Q6	XSTR, SI, PNP	195974	04713	2N3906	1	1	
R1	RES, WW, 0.2 +/-3%, 0.7W	255661	89536	255661	1		
R2	RES, MTL. FILM, 1.1K +/-1%, 1/8W	241497	91637	CMF551101F	1		
R4	RES, DEP. CAR, 100K +/-5%, 1/4W	348920	80031	CR251-4-5P100K	1		
R5	RES, MTL. FILM, 86.6K +/-1%, 1/8W	291468	91637	CMF558661F	1		
R6	RES, DEP. CAR, 47 +/-5%, 1/4W	441592	80031	CR251-4-5P47E	2		
R7	RES, MTL. FILM, 61.9K +/-1%, 1/8W	237230	91637	CMF556191F	1		
R8	RES, MTL. FILM, 249K +/-1%, 1/8W	268805	91637	CMF552493F	1		
R9	RES, DEP. CAR, 1.2K +/-5%, 1/4W	441378	80031	CR251-4-5P1K2	1		
R10	RES, DEP. CAR, 47 +/-5%, 1/4W	441592	80031	CR251-4-5P47E	REF		
R11	RES, COMP, 10 +/-5%, 1W	166298	01121	GB1005	1		
R12	RES, DEP. CAR, 330 +/-5%, 1/4W	368720	80031	CR251-4-5P330E	1		
R13	RES, DEP. CAR, 82 +/-5%, 1/4W	442277	80031	CR251-4-5P82E	1		
R14	RES, MTL. FILM, 10K +/-1%, 1/8W	168260	91637	CMF551002F	1		
R15	RES, MTL. FILM, 6.65K +/-1%, 1/8W	294918	91637	CMF556651F	1		
R16	RES, THERMISTOR, 10K +/-10%, 3 MW	104596	15801	JA41J1			
R17	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	REF		
R18	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-4-5P470E	1		
T1	XFMR, POWER	486530	89536	486530	1		
U1	IC, LINEAR OP AMP	414284	12040	LM1458N	1	1	
U2⊘	IC, COS/MOS, NOR GATES, POS LOGIC	355172	02735	CD4001AE	1	1	
W1	CABLE, BATTERY #1	488403	89536	488403	1		
W2	CABLE, BATTERY #2	488411	89536	488411	1		
W3	CABLE, BATTERY #3	491704	89536	491704	1		

NOTE: ⊘ Indicates the item can be damaged by static discharge.

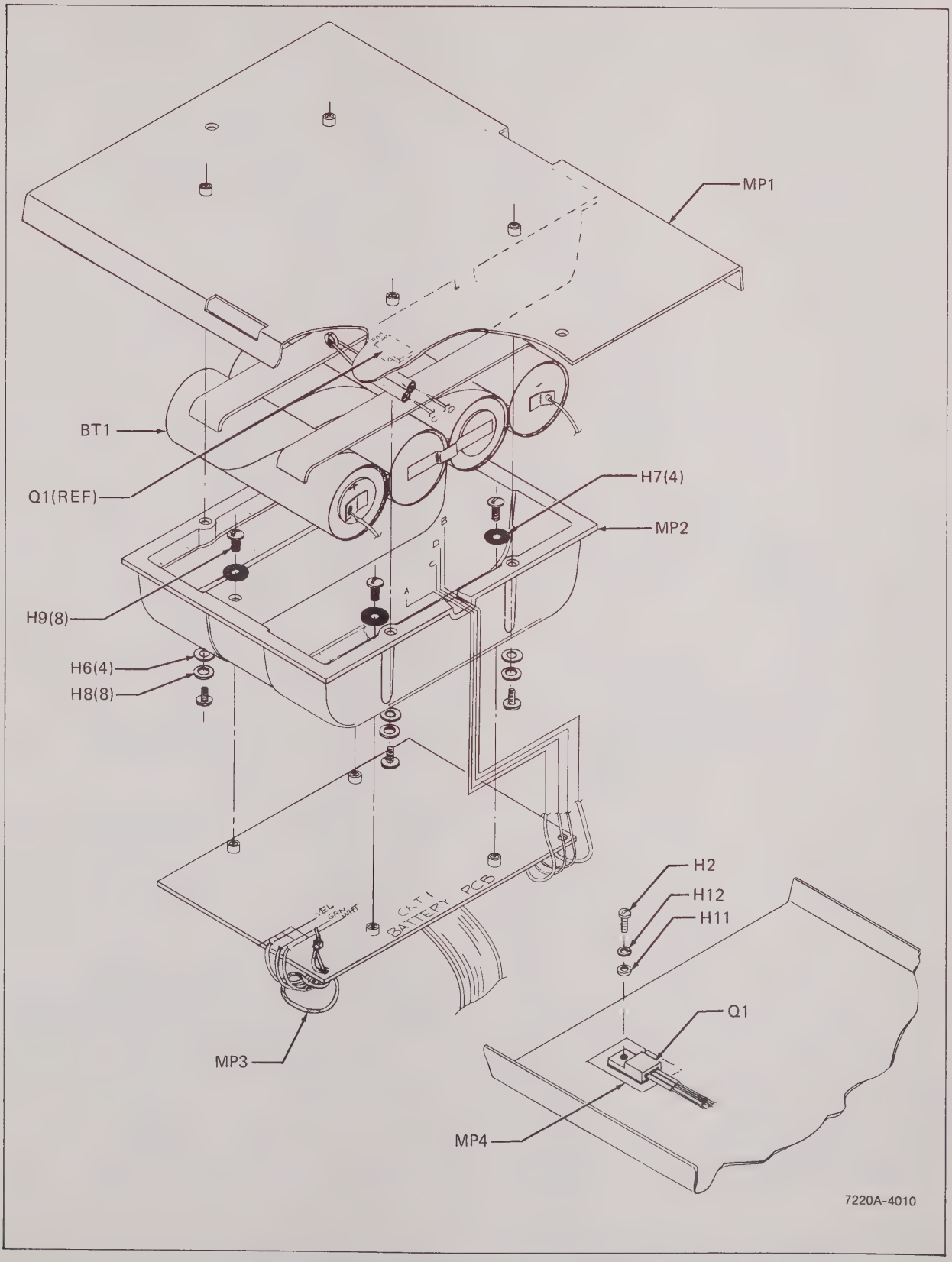


Figure 010-3. Battery Option -010 Assembly

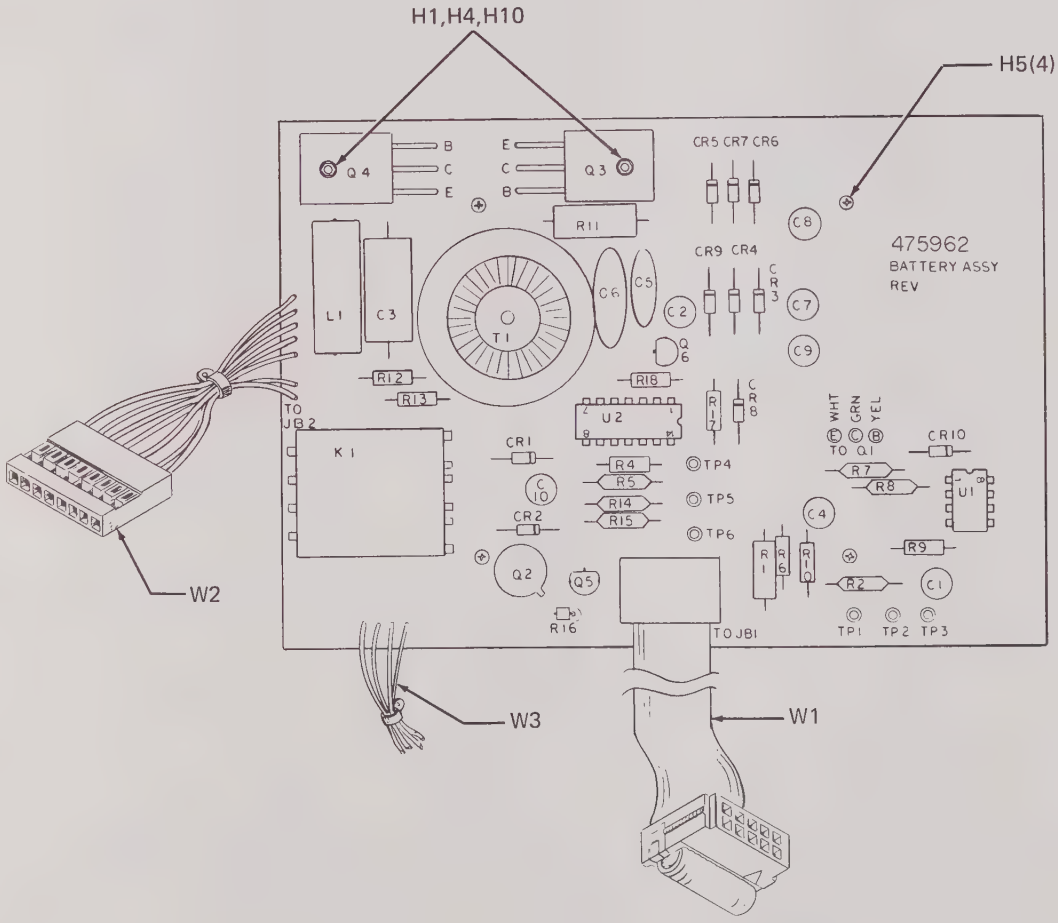


Figure 010-3. Battery Option -010 Assembly (cont)

Option-112
2 PPM TCXO

6112-1. INTRODUCTION

6112-2. Option -112 is a temperature compensated crystal oscillator (TCXO) with an intrinsic stability greater than the standard time base. This increased stability is due to a temperature compensation network. Figure 6112-1 shows the frequency variation for change in temperature for an uncompensated oscillator and the compensation network effect. The resulting frequency deviation (solid line) is held to a minimum over the designated temperature range. If the temperature limits are exceeded, the time base stability may exceed the specified value.

6112-3. SPECIFICATIONS

6112-4. Specifications of the 72XXA-112 Option are listed in Table 6112-1. Comparative specifications for the other time bases available are listed in Section 1.

6112-5. INSTALLATION

6112-6. Installation of the 2 PPM TCXO (Option -112) necessitates removal of the counter's Main PCB; refer to disassembly instructions in Section 4. For each counter, the TCXO is installed in the left rear corner of the Main PCB. Use the following installation procedure:

1. Unsolder and remove any other time base already installed.

2. Referring to Figure 6112-2, install the TCXO and the insulator.

3. While exercising care not to overheat the Main PCB, solder the TCXO connections.

4. Complete jumper and solder bridge arrangements as described below:

a. 7250A: Ensure that solder bridge SB2 is not shorted (bottom of Main PCB, left front corner). Also remove any jumper between W1 and +5V, and jumper W1 to +12V (top of Main PCB, left front corner).

b. 7260A or 7261A: If necessary, remove the shorts on solder briges SB2 (bottom of Main PCB, left front corner) and SB4 (bottom, left rear). Jumper SB5 (left rear, next to SB4) to the immediately adjacent side of SB4.

6112-7. OPERATION

6112-8. Operation of the instrument with the -112 Option installed is the same as operation of a standard instrument. Refer to Section 2 for operating instructions.

6112-9. CALIBRATION

6112-10. Calbration for the TCX0 (Option -112) time base necessitates the use of a frequency reference with an accuracy of $\pm 1 \times 10^{9}$. A cesium standard, such as the HP 5061A, is recommended. This calibration procedure calls for applying the reference frequency to Channel A and adjusting the time base for a counter display of the known input. At the 0.1 Hz RESOLUTION setting on the counter, this method yields an adjustable accuracy of ±5 parts in 108 (± one count error). Proceed with the following steps:

1. Ensure that the counter's top and bottom covers are installed.

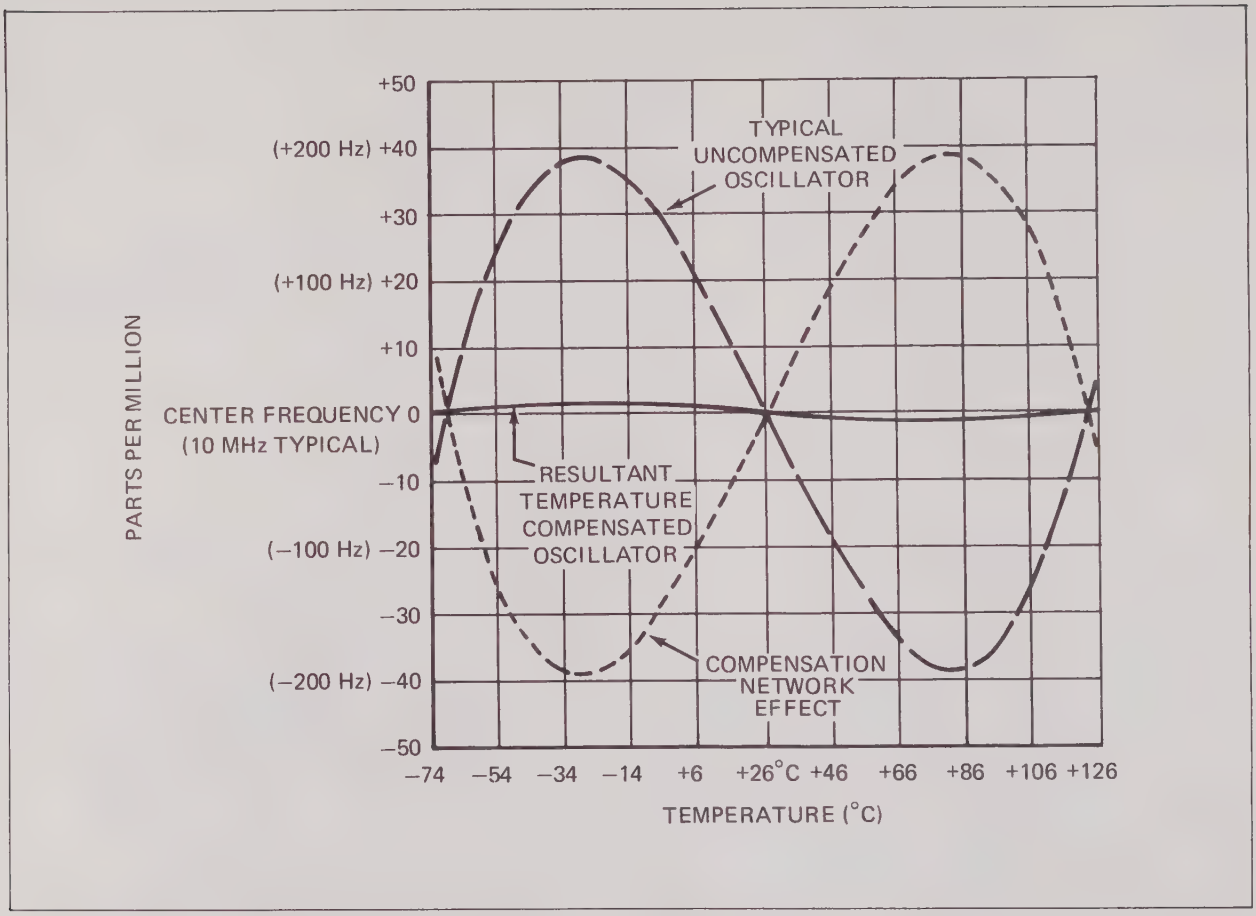


Figure 6112-1. Compensation Effects

Table 6112-1. Option 72XXA-112 Specifications

Nominal Frequency	10 MHz
Aging Rate	$\pm 3 \times 10^{-7}$/month
	$\pm 1 \times 10^{-6}$/year
Accuracy with Temperature (0° to 50°C) .	$\pm 2 \times 10^{-6}$
Line Voltage . . . . . (10% line variation)	$\pm 2 \times 10^{-8}$
Battery Operation	$\pm 2 \times 10^{-8}$

2. Apply power to the counter and allow for a minimum warmup of 2 hours.

3. Set counter controls and connections as defined in Section 4 of this manual ("Time Base Calibration").

4. Connect the 5 MHz (100 mV) frequency reference output to CHANNEL A input on the counter.

5. If necessary, adjust the time base so that the counter's display corresponds to the first reading presented in Table 6112-2. The adjustment is accessed through a hole in the left rear corner of the bottom case half. Use a JFD 5284 (or equivalent) non-ferrous adjustment tool. If installed at the rear of the bottom case half, the bail will have to be removed to allow access.

6. Change the counter's RESOLUTION setting to the next step listed in Table 6112-2 and repeat step (5) for the respective display. Display update in the 0.1 Hz setting occurs every 10 seconds.

NOTE

When the OVFL LED is illuminated, observed the GATE LED (on) to verify that a measurement is being made.

Table 6112-2. Calibration

RESOLUTION	DISPLAY (±2 COUNT)
1 Hz	5000.000 kHz (7250A, 7260A, 7261A)
0.1 Hz	000.0000 kHz* (7250A) 5000.0000 kHz (7260A, 7261A)

6112-11. REPLACEABLE PARTS

6112-12. The 72XX-112 Option is a completely sealed unit containing no replacement parts. A replacement can be ordered by using Fluke Part Number 516138. The insulator can be ordered seperately by using Fluke Part Number 487710.

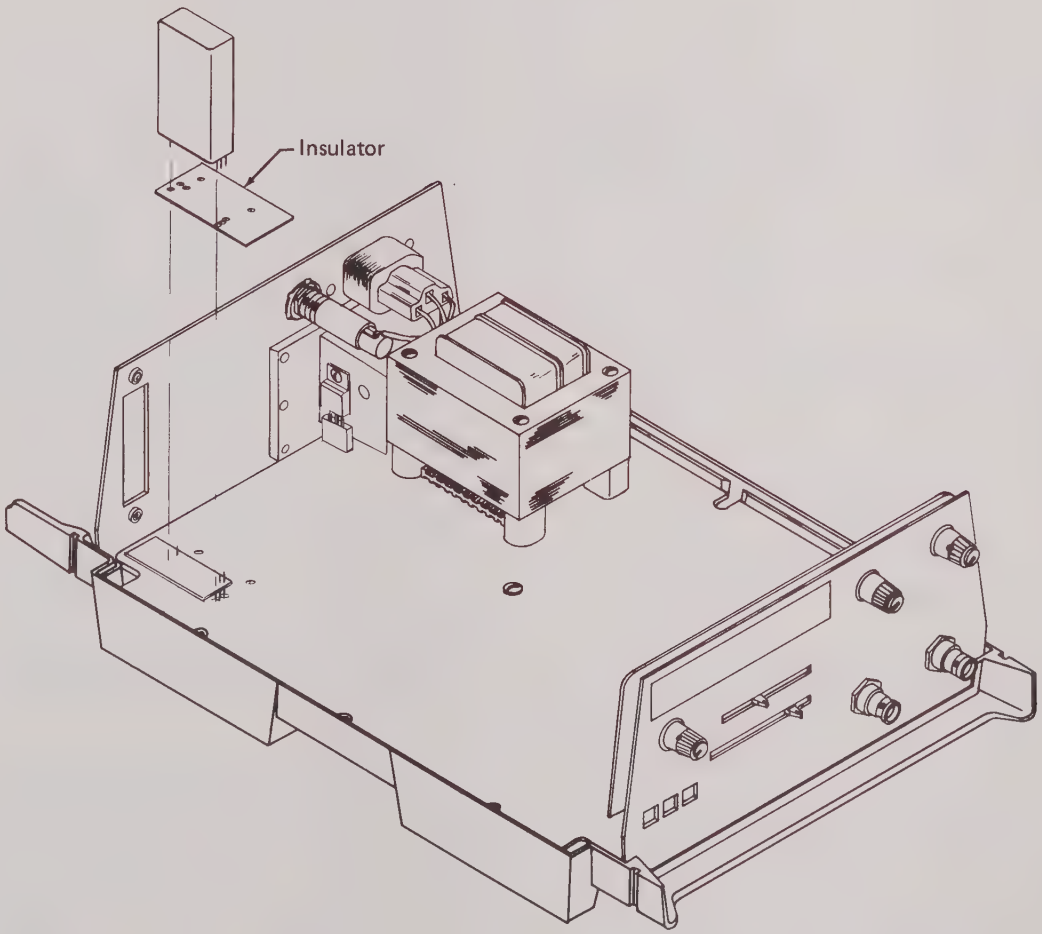


Figure 6112-2. Installation

Option-131
Low Power Oven Time Base

131-1. INTRODUCTION

131-2. The -131 Option is a crystal oscillator inside a temperature stabilized oven. The oven uses an extremely small amount of power. After the assembly is warmed up, power consumption is 1 watt, typically. This allows oven controlled time base accuracy with a battery powered instrument. Operation and Calibration of an instrument equipped with the -131 Option is the same as with a standard instrument. Refer to Sections 2 and 4 of this manual for additional information.

131-3. SPECIFICATIONS

131-4. The specifications of the -131 Option are listed in Table 131-1.

131-5. INSTALLATION

6131-6. Installation of the Low Power Oven Time Base (Option -131) necessitates removal of the counter's Main PCB; refer to disassembly instructions included with Section 4. For each counter, the Low Power Oven Time Base is installed in the top left rear corner of the Main PCB. Use the following installation procedure:

1. Unsolder and remove any other time base already installed.

2. Referring to Figure 131-1, install the Low Power Oven Time Base and insulator. Use the provided hardware to secure the time base to the Main PCB.

3. While exercising care not to overheat the Main PCB, solder the time base connections.

4. Complete jumper and solder bridge arrangements on the Main PCB as described below:

a. 7220A: If necessary, remove the short at SB4 and jumper SB5 (bottom of Main PCB, left rear corner). Jumper SB2 (bottom, left front corner).

b. 7250A: If necessary, remove the short between W1 and +12V and jumper W1 to +5V (top of Main PCB, left front corner). Jumper SB2 (bottom of Main PCB, left front corner).

c. 7260A or 7261A: Remove the short at SB5 and jumper SB4 (bottom of Main PCB, left rear). Jumper SB2.

Table 131-1. -131 Option Specifications

Nominal Frequency	10 MHz
Aging Rate	1×10^{-7}/month*
Accuracy with Temperature (0° to 40°C)	$\pm 1 \times 10^{-7}$
Line Voltage (10% line variation)	2×10^{-8}
Warmup**	
10 minutes	5×10^{-7}
20 minutes	3×10^{-8}
Battery Operation	$\pm 5 \times 10^{-8}$

* After 5 days continuous operation.

** Specifies offset from final frequency value (the value after 24 hours).

131-7. CALIBRATION

131-8. Calibration for the Low Power Oven Time Base necessitates the use of a frequency reference with an accuracy of $\pm 1 \times 10^{-9}$. A cesium standard, such as the HP

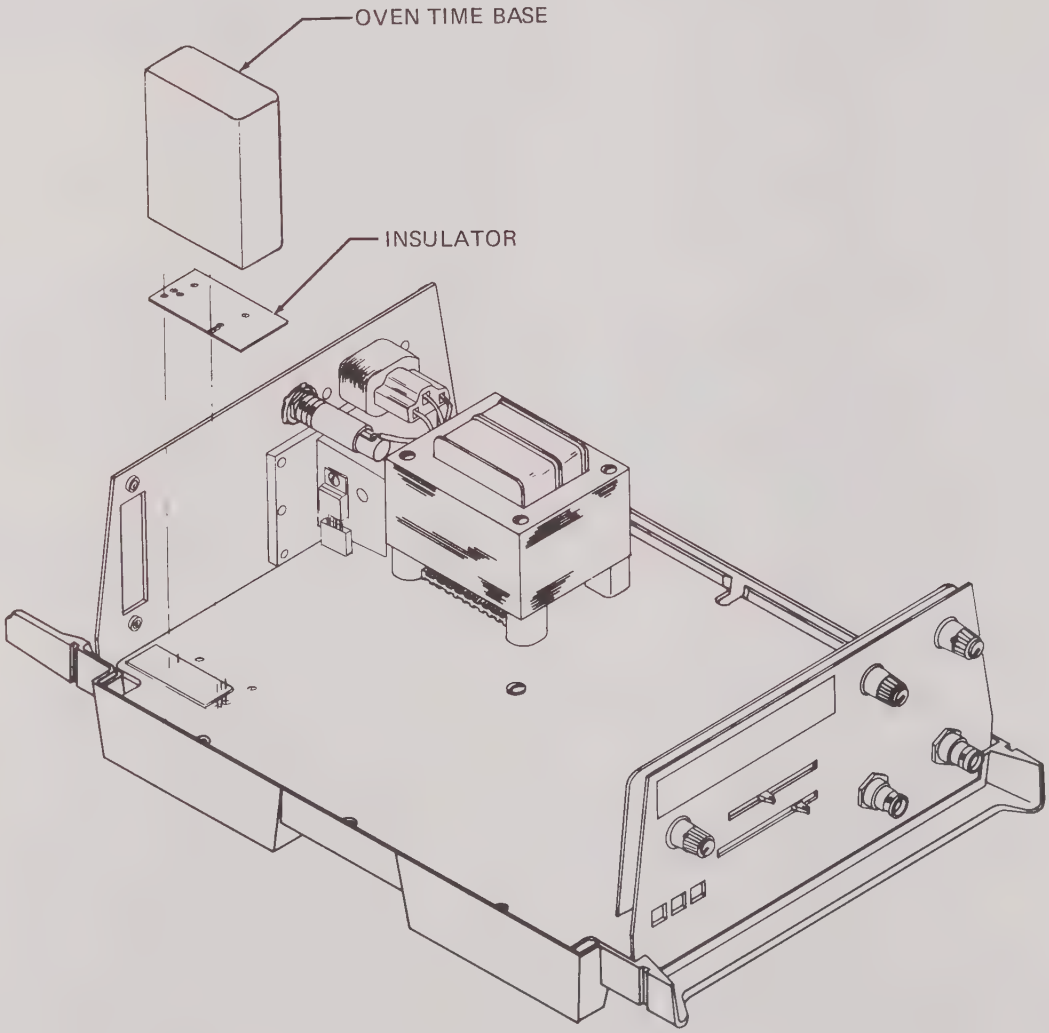


Figure 131-2. Installation

5061A, is recommended. This calibration procedure calls for applying the reference frequency to Channel A and adjusting the time base for a counter display of the known input. At the 0.1 Hz RESOLUTION setting on the counter, this method yields an adjustable accuracy of 2 parts in 10^8 (± one count error). Proceed with the following steps:

1. Ensure that the counter's top and bottom covers are installed.

2. Apply power to the counter and allow for a minumum warmup of 20 minutes. When possible a warmup of 24 hours is preferred.

3. Set counter controls and connections as defined in Section 4 of this manual ("Time Base Calibration").

4. Connect the 5 MHz (100 mV) frequency reference output to CHANNEL A input on the counter.

5. If necessary, adjust the time base so that the counter's display corresponds to the first reading presented in Table 6131-2. The adjustment is accessed through a hole in the left rear corner of the bottom case half. Use a JFD 5284 (or equivalent) non-ferrous adjustment tool. If installed at the rear of the bottom case half, the bail will have to be removed to allow access.

6. Change the counter's RESOLUTION setting to the next step listed in Table 6131-2 and repeat step (5) for the respective display. Display update in the 0.1 Hz setting occurs every ten seconds.

NOTE

When the OVFL LED is illuminated, observe the GATE LED (on) to verify that a measurement is being made.

6131-9. LIST OF REPLACEABLE PARTS

131-10. A replacement oscillator can be ordered by using Fluke Part Number 516112. The Manufacturer's Federal Supply Code is 89536 and the Manufacturer's Part Number is 516112. The insulator can be ordered with part number 487710. Refer to Section 5 for ordering information.

Table 131-2. Calibration

RESOLUTION	DISPLAY (±1 COUNT)
1 Hz	5000.000 kHz (7250A, 7260A, 7261A) 5.000000 MHz (7220A)
0.1 Hz	000.0000 kHz* (7250A) 5000.0000 kHz (7260A, 7261A) 5.0000000 MHz (7220A)

Option -132
Superior Low Power Oven Time Base

132-1. INTRODUCTION

132-2. The -132 Option is a crystal oscillator inside a temperature stabilized oven. The oven uses an extremely small amount of power. After the assembly is warmed up, power consumption is 1 watt, typically. This allows oven controlled time base accuracy with a battery powered instrument. Operation and Calibration of an instrument equipped with the -132 Option is the same as with a standard instrument. Refer to Sections 2 and 4 of this manual for additional information.

132-3. SPECIFICATIONS

132-4. The specifications of the -132 Option are listed in Table 132-1.

132-5. INSTALLATION

132-6. Installation of the Superior Low Power Oven Time Base (Option -132) necessitates removal of the counter's Main PCB; refer to disassembly instructions included with Section 4. For each counter, the Superior Low Power Oven Time Base is installed in the top left rear corner of the Main PCB. Use the following installation procedure:

1. Unsolder and remove any other time base already installed.

2. Referring to figure 132-1, install the Superior Low Power Oven Time Base and insulator. Use the provided hardware to secure the time base to the Main PCB.

3. While exercising care not to overheat the Main PCB, solder the time base connections.

4. Complete jumper and solder bridge arrangements on the Main PCB as described below:

a. 7220A: If necessary, remove the short at SB4 and jumper SB5 (bottom of Main PCB, left rear corner). Jumper SB2 (bottom, left front corner).

b. 7250A: If necessary, remove the short between W1 and +12V and jumper W1 to +5V (top of Main PCB, left front corner). Jumper SB2 (bottom of Main PCB, left front corner).

c. 7260A or 7261A: Remove the short at SB5 and jumper SB4 (bottom of Main PCB, left rear). Jumper SB2.

Table 132-1. -132 Option Specifications

Nominal Frequency	10 MHz
Aging Rate	$\pm 3 \times 10^{-9}$/day*
	$\pm 5 \times 10^{-8}$/month*
Accuracy with Temperature (0° to 40°C)	$\pm 3 \times 10^{-8}$
Line Voltage (10% line variation)	$\pm 4 \times 10^{-9}$
Warmup	
10 minutes	$\pm 5 \times 10^{-7}$
20 minutes	$\pm 3 \times 10^{-8}$
Battery Operation	$\pm 1 \times 10^{-8}$

* After 5 days continuous operation.
** Specifies offset from final frequency value (the value after 24 hours).

132-7. CALIBRATION

132-8. Calibration for the Superior Low Power Oven Time Base necessitates the use of a frequency reference

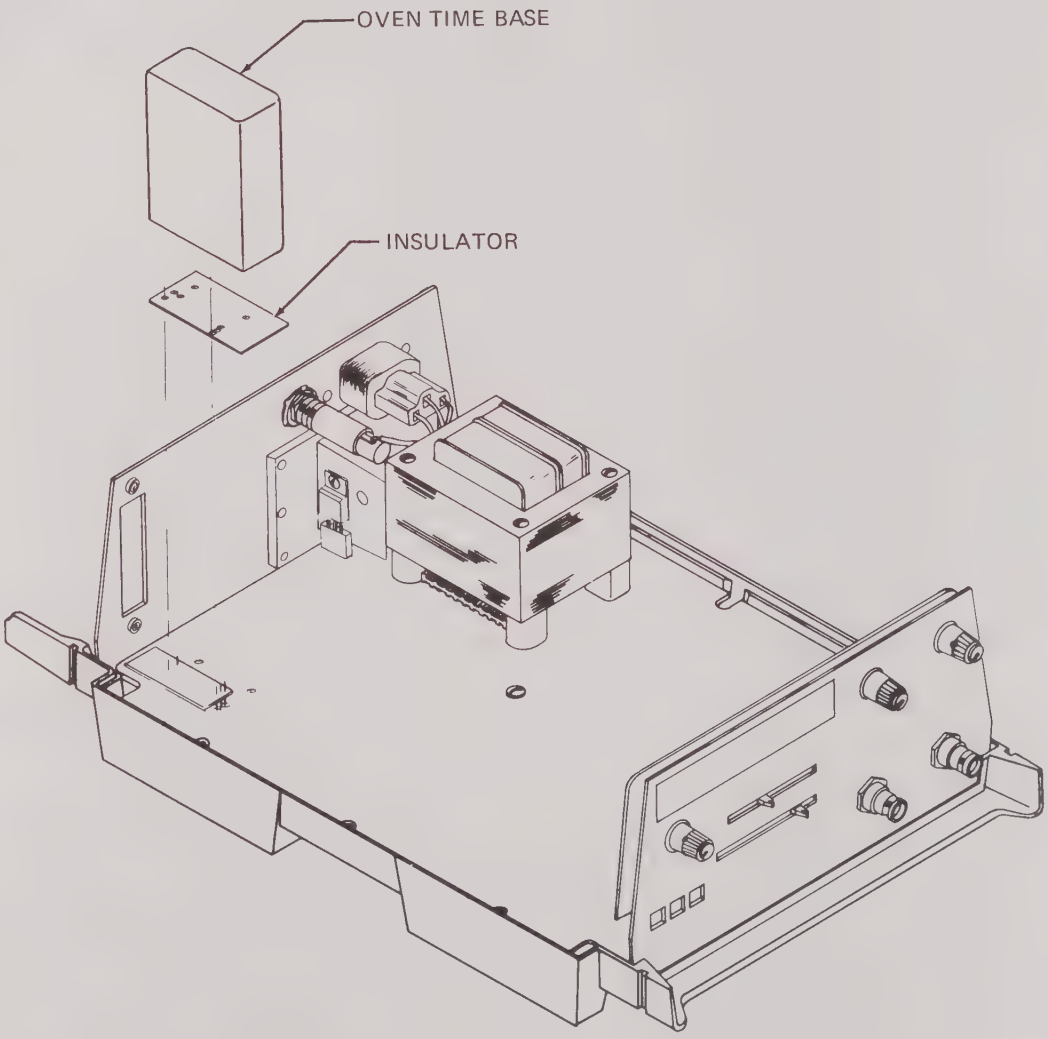


Figure 132-1. Installation

with an accuracy of ±1 X 10^9. A cesium standard, such as the HP 5061A, is recommended. This calibration procedure calls for applying the reference frequency to Channel A and adjusting the time base for a counter display of the known input. At the 0.1 Hz RESOLUTION setting on the counter, this method yields an adjustable accuracy of 2 parts in 10^8 (±1 count error). Proceed with the following steps:

1. Ensure that the counter's top and bottom covers are installed.

2. Apply power to the counter and allow for a minumum warmup of 20 minutes. When possible a warmup of 24 hours is preferred.

3. Set counter controls and connections as defined in Section 4 of this manual ("Time Base Calibration").

4. Connect the 5 MHz (100 mV) frequency reference output to CHANNEL A input on the counter.

5. If necessary, adjust the time base so that the counter's display corresponds to the first reading presented in Table 132-2. The adjustment is accessed through a hole in the left rear corner of the bottom case half. Use a JFD 5284 (or equivalent) nonferrous adjustment tool. If installed at the rear of the bottom case half, the bail will have to be removed to allow access.

6. Change the counter's RESOLUTION setting to the next step listed in Table 132-2 and repeat step (5) for the respective display. Display update in the 0.1 Hz setting occurs every ten seconds.

NOTE

When the OVFL LED is illuminated, observe the GATE LED (on) to verify that a measurement is being made.

132-9. LIST OF REPLACEABLE PARTS

132-10. A replacement oscillator can be ordered by using the Fluke Part Number 516096. The Manufacturer's Federal Supply Code is 89536 and the Manufacturer's Part Number is 516096. The insulator can be ordered with Fluke Part Number 487710. Ordering information is given in Section 5 of the Instruction Manual.

Table 6132-2. Calibration

RESOLUTION	DISPLAY (±1 COUNT)
1 Hz	5000.000 kHz (7250A, 7260A, 7261A) 5.000000 MHz (7220A)
0.1 Hz	000.0000 kHz* (7250A) 5000.0000 kHz (7260A, 7261A) 5.0000000 MHz (7220A)

-310 Option
520 MHz Direct

6310-1. INTRODUCTION

6310-2. The -310 Option can directly measure the frequency of signals from 50-520 MHz. The option uses the Channel C input terminal. There are no controls for this channel. Input impedance is 50Ω to improve VSWR. The input is fuse protected by F1 on the 520 MHz Direct PCB. A spare fuse is provided on the pcb.

6310-3. OPERATION

6310-4. To use the -310 Option, set the FUNCTION control on the Front Panel of the instrument to the FREQ C position. Connect the unknown signal to the Channel C input terminal. Set the RESOLUTION control to the desired range.

6310-5. THEORY OF OPERATION

6310-6. As Figure 610-1 shows, the 520 MHz Direct PCB conditions the input signal on Channel C and provides a high speed counter for the first decade of counting. The input signal applied to the Channel C terminal is ac-coupled and fuse protected to the input of the signal conditioner. As the FUNCTION switch is moved to the FREQ C position, the instrument generates a general Reset pulse that also reset the Sync Gate and first decade counter on the 520 MHz Direct PCB. When the FUNCTION switch is in the FREQ C position, the logic terms FC and $\overline{FC}$ are decoded by the Function ROM U42 on the Main PCB. FC and $\overline{FC}$ work together to select the proper Main Gate Enable logic, timing logic, control logic, turn off the Channel A and Channel B Signal Conditioners, and (through K1) turn on the 520 MHz Direct PCB. The signal input on Channel C is processed through the signal conditioner and applied to the first decade counter, U2, (a special high speed counter) and to the Threshold Detection Circuit. If the amplitude of the signal applied to the Channel C input is above 8 mV rms (approximately), the Threshold Detector will enable the Sync Gate and 1st Decade Counter. Should the amplitude of the Channel C input fall below 6 mV rms (approximately), the Threshold Detector immediately disables the Sync Gate and 1st Decade Count. The measurement is stopped. When the instrument generates $\overline{GQ}$, the 100 kHz signal from the time base dividers acting through the sync gate on the 520 MHz Direct PCB, enables the first decade counter. The carry output of the first decade counter (5-50 MHz) is routed through the Clock Select on the Main PCB to the first decade counter on the Main PCB. This counter is used to count the second decade for FREQ C measurements (it normally counts signals up to 125 MHz) the second decade counter on the Main PCB is bypassed. This is accomplished by the $\overline{C\ DIRECT}$ signal (a ground) from the 520 MHz Direct PCB being ANDed with $\overline{FC}$. The resulting logic term disqualifies the MUX on the Main PCB and qualifies the MUX on the 520 MHz Direct PCB. The outputs of the first decade counter on the 520 MHz Direct PCB (first decade) and the output of the first decade counter on the Main PCB (second decade) are routed through the MUX on the 520 MHz Direct PCB to the counter, U15, on the Main PCB and from there to the Display as usual.

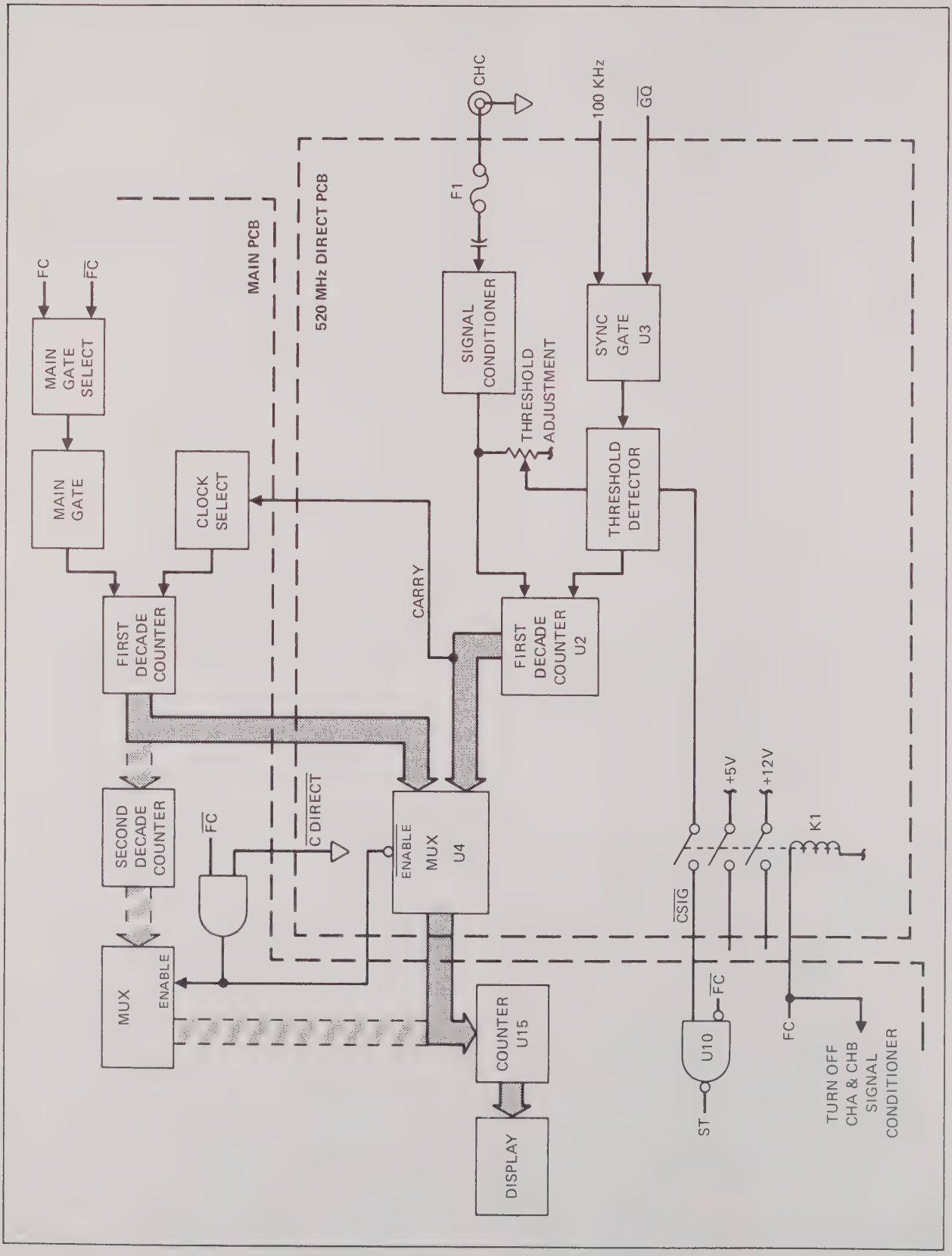


Figure 6310-1. 520 MHz Direct Basic Block Diagram

6310-7. INSTALLATION

6210-8. As Figure 6310-2 shows, the option includes both the 520 MHz Direct PCB and the Channel C input cable. Use the following procedure to install the option:

1. Set the AC POWER switch to the OFF position and remove the line power cord.

2. Using the Disassembly procedure given in Section 4, remove the Front Panel Assembly, then:

a. As shown in Figure 6310-3, unscrew the Front Panel PCB from the Front Panel.

b. Remove the plug button from the Channel C input terminal hold.

c. Mount the BNC plug of the Channel C cable.

WARNING

MAKE SURE THAT THE NUT (SHOWN AS FLAG C) FLAT IS PARALLEL WITH THE BOTTOM OF THE FRONT PANEL OR IT WILL INTERFERE WITH THE SLIDE SWITCHES.

d. Mount the BNC insert using the large nut.

e. Fasten the Front Panel PCB to the the Front Panel.

f. Reconnect the Front Panel Assembly to the Main PCB.

3. Fasten the Channel C cable to the connector on the 520 MHz Direct PCB.

4. Plug the 520 MHz Direct PCB into P6 on the Main PCB.

5. Mount the Main PCB onto the bottom case cover of the instrument.

6. Mount the top case cover of the instrument.

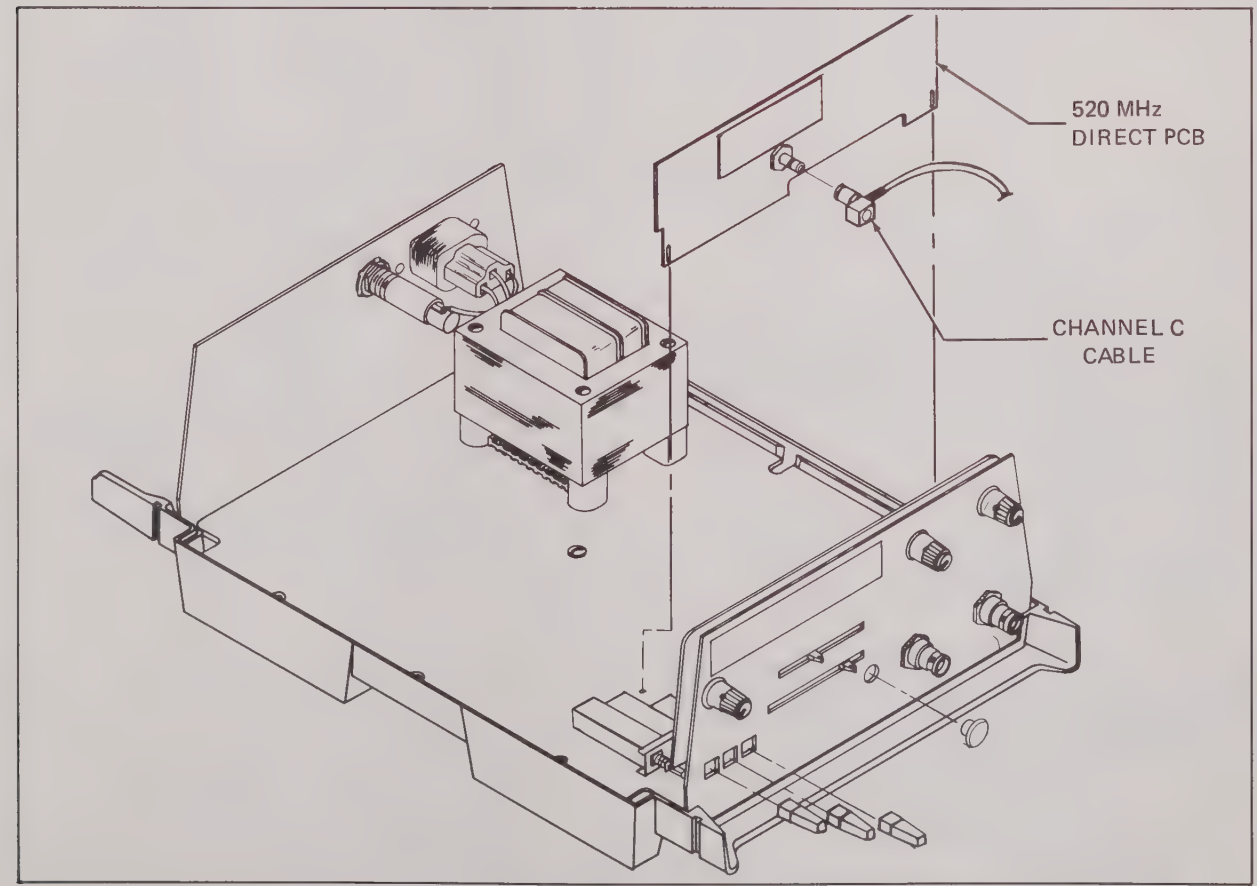


Figure 6310-2. Installation - I

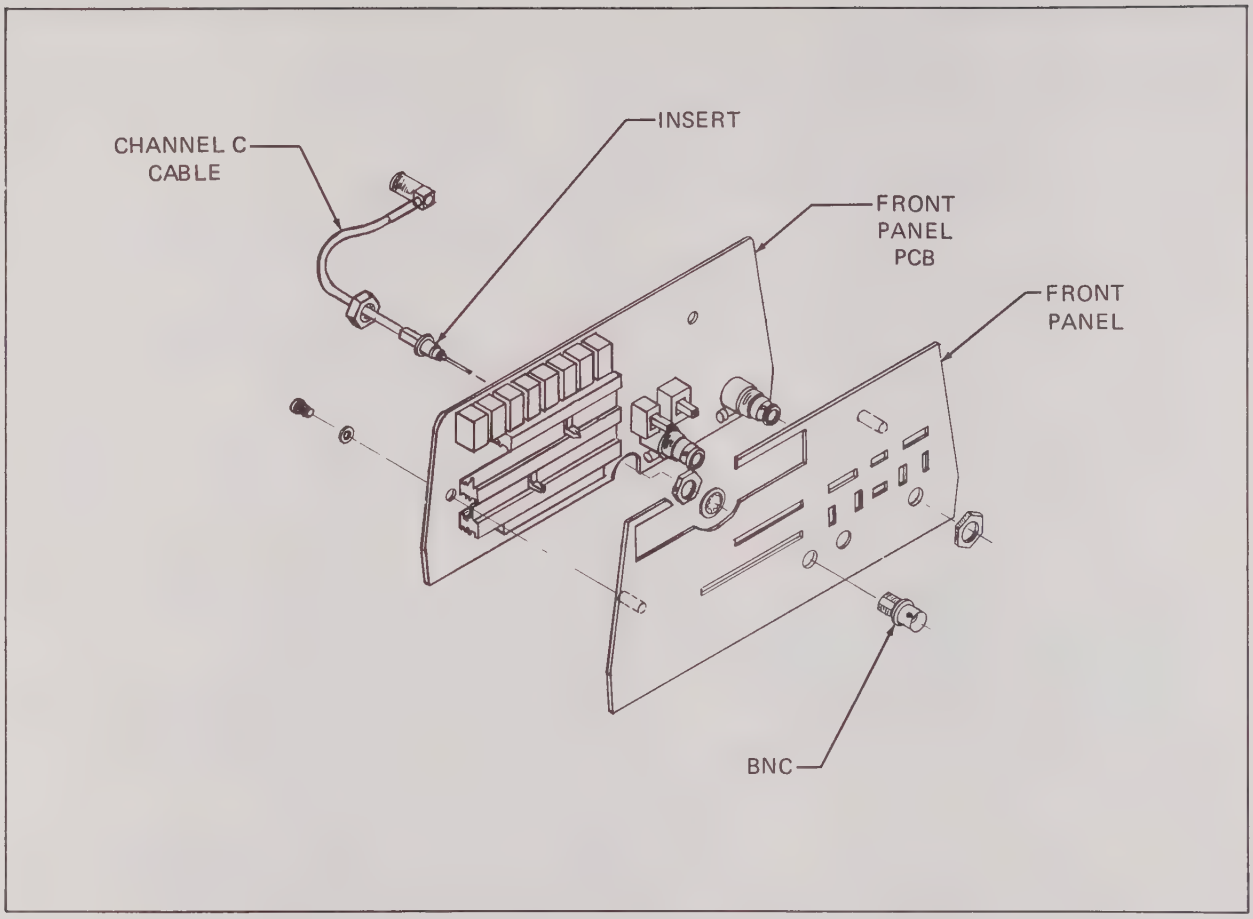


Figure 6310-3. Installation - II

6310-9. Fuse Replacement

6310-10. The input protection fuse F1 is a special fast blow fuse. Should the fuse fail, a spare is provided on the 520 MHz Direct PCB and is labeled F2. Should both fuses fail, replace them with the fuse specified in the List of Replaceable Parts (Table 6310-2).

6310-11. PERFORMANCE CHECK

6310-12. Use the HP 8660B Signal Generator (with 11661B) and the following procedure to check the performance of the 520 MHz Direct PCB.

1. Set the Front Panel controls of the instrument to the following positions:

FUNCTION	- FREQ C
RESOLUTION	- 10 Hz

2. Set the Rear Panel controls to the following positions:

REF	- EXT
MODE	- CONT

3. Connect the the equipment as shown in Figure 6310-4.

4. Program the Signal Generator for the output frequencies listed in Table 6310-1 at the following levels into the UUT:

   a. 10 mV rms.

   b. 10 dB down from the level in a.

5. Verify that the UUT display:

   a. In 4a, agrees with the frequency programmed into the Signal Generator for each step of Table 6310-1.

   b. In 4b, goes to all zeros.

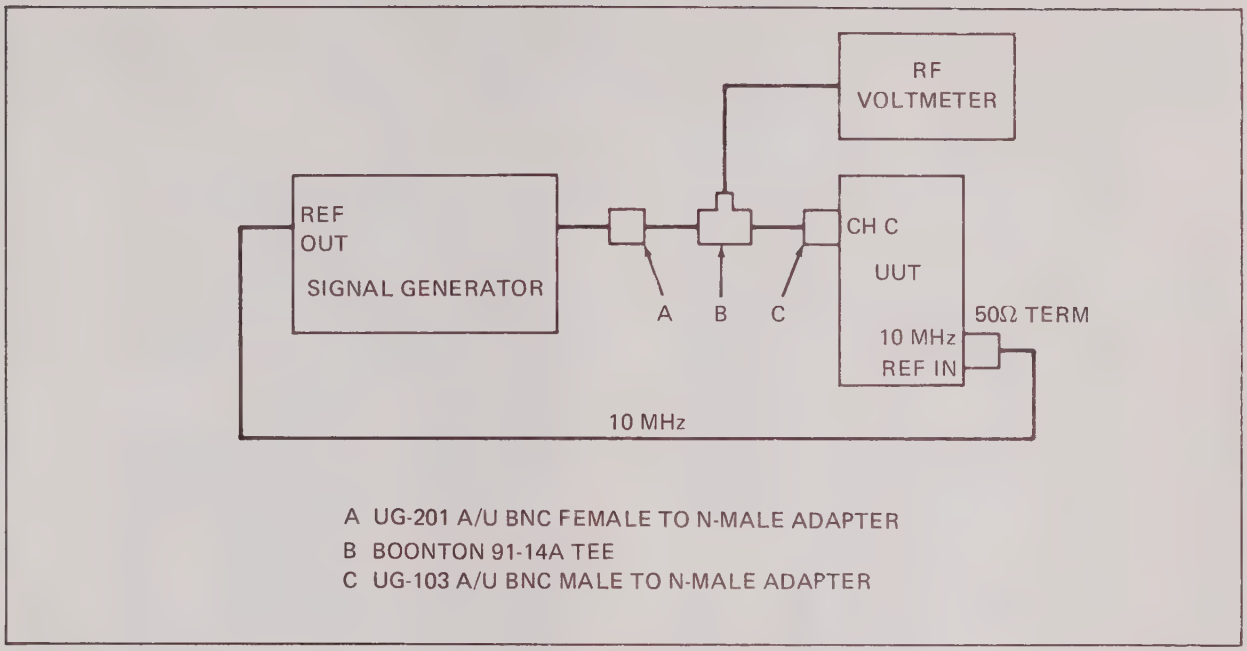


Figure 6310-4. Frequency C Check

Table 6310-1. Performance Check

PROGRAMMED FREQUENCY (in MHz)	DISPLAY (in kHz)	ERROR (in COUNTS)
50	50000.00	
100	100000.00	
150	150000.00	
200	200000.00	
250	250000.00	
300	300000.00	±1
350	350000.00	
400	400000.00	
450	450000.00	
500	500000.00	
520	520000.00	

6310-13. Threshold Adjustment

6310-14. Use the following procedure to set the Threshold Adjustment to the proper value:

1. Perform steps 1 and 2 of the Performance Check.

2. Program the Signal Generator for an input to the UUT of 250 MHz at a level of 7 mV rms.

3. Adjust the Threshold Adjust (R23) for a stable display with the GATE light flashing.

4. Verify that the UUT display is 250000.00 kHz ±1 count.

5. If the adjustment cannot be made, reprogram the Signal Generator for a higher level. If the adjustment cannot be made with the HF synthesizer programmed for an output level of 10 mV rms or less, troubleshooting and repair is indicated.

6310-15. LIST OF REPLACEABLE PARTS

6310-16. Table 6310-2 is a list of replaceable parts for the -310 Option. Figure 6310-5 is a component location diagram of the 520 MHz Direct PCB.

Table 6310-2. Direct Channel C Assembly, 520 MHz

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	NOTE
-310	DIRECT CHANNEL C ASSEMBLY, 500MHZ FIGURE 6310-5 (7260A-4003T)	ORDER	BY	OPTION -310			
C1	CAP, TA, 68 UF +/-20%, 15V	193615	56289	196D686X0015TE4	1		
C2	CAP, TA, 47 +/-20%, 20V	348516	56289	196D476X0020TE4	1		
C3	CAP, TA, 22 UF +/-20%, 20V	161331	56289	196D226X0035HA1	3		
C4	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	6		
C5	CAP, TA, 20 UF +/-20%, 20V	161927	56289	196D2225X0020HA1	1		
C6	CAP, MICA, 82 +/-5%, 500V	148502	72136	DM15F820J	1		
C8	CAP, CER, .001 UF +/-20%, 100V	402966	32897	8121-A100-W5R-102M	4		
C9	CAP, CER, .001 UF +/-20%, 100V	402966	32897	8121-A100-W5R-102M	REF		
C10	CAP, CER, .01 UF +/-20%, 100V	407361	32897	8121-A100-W5R-103M	1		
C11	CAP, CER, .001 UF +/-20%, 100V	402966	32897	8121-A100-W5R-102M	REF		
C12	CAP, CER, .001 UF +/-20%, 100V	402966	32897	8121-A100-W5R-102M	REF		
C13	CAP, TA, 22 UF +/-20%, 35V	161331	56289	196D226X0035HA1	REF		
C14	CAP, TA, 22 UF +/-20%, 35V	161331	56289	196D226X0035HA1	REF		
C15	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C16	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C17	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C18	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C19	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
CR1	DIODE, ZENER	246611	07910	1N960B	1	1	
CR2	DIODE, HOT CARRIER	369595	07263	FH1100	4	1	
CR3	DIODE, HOT CARRIER	369595	07263	FH1100	REF		
CR4	DIODE, HOT CARRIER	369595	07263	FH1100	REF		
CR5	DIODE, HOT CARRIER	369595	07263	FH1100	REF		
CR6	DIODE, SI, HI-SPEED SWITCH	203323	09214	IN4448	4	1	
CR7	DIODE, SI, HI-SPEED SWITCH	203323	09214	IN4448	REF		
CR8	DIODE, SI, HI-SPEED SWITCH	203323	09214	IN4448	REF		
CR9	DIODE, SI, HI-SPEED SWITCH	203323	09214	IN4448	REF		
F1	FUSE, 1/4 AMP	370577	75915	273.200	2	10	
F2	FUSE, 1/4 AMP	370577	75915	273.200	REF		
J2	CONNECTOR, BNC	352450	98291	51-051-0000	1		
J11	SOCKET, BERG, PCB MOUNTING, 40-PIN	376418	22526	75060-007	40		
K1	RELAY, DRY REED	494732	21317	E544X5	1		
L1	CHOKE, 6-TURN	320911	89536	320911	2		
L2	CHOKE, 6-TURN	320911	89536	320911	REF		
MP1	CONNECTOR, RECEPTACLE, BOARD MOUNT	375329	00779	85863-3	2		
MP2	CONNECTOR, SMA	352450	98291	51-051-0000	1		
Q1	XSTR, SI, NPN, HI-SPEED SATURATED SWITCH	369645	07263	2N4274	1	1	
Q2	XSTR, SI, NPN	218396	04713	2N3904	2	1	
Q3	XSTR, SI, NPN, DARLINGTON TO-92	381798	12040	MPS A-13	1	1	
Q4	XSTR, SI, NPN	218396	04713	2N3904	REF		
R1	RES, DEP. CAR, 10K +/-5%, 1/4W	348839	80031	CR251-4-5P10K	5		
R2	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-4-5P470E	3		
R3	RES, DEP. CAR, 1.8K +/-5%, 1/4W	441444	80031	CR251-4-5P1K8	2		
R4	RES, DEP. CAR, 1.8K +/-5%, 1/4W	441444	80031	CR251-4-5P1K8	REF		
R5	RES, DEP. CAR, 5.1K +/-5%, 1/4W	368712	80031	CR251-4-5P5K1	1		
R6	RES, DEP. CAR, 10K +/-5%, 1/4W	348839	80031	CR251-4-5P10K	REF		
R7	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	1		

Table 6310-2. Direct Channel C Assembly, 520 MHz (cont)

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE		TOT QTY	REC QTY	NOTE
R8	RES, DEP. CAR, 10K +/-5%, 1/4W	348839	80031	CR251-4-5P10K	REF		
R9	RES, DEP. CAR, 160K +/-5%, 1/4W	442442	80031	CR251-4-5P160K	1		
R10	RES, DEP. CAR, 10K +/-5%, 1/4W	348839	80031	CR251-4-5P10K	REF		
R11	RES, DEP. CAR, 180K +/-5%, 1/4W	348946	80031	CR251-4-5P180K	2		
R12	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-4-5P470E	REF		
R13	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-4-5P4K7	1		
R14	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-4-5P470E	REF		
R15	RES, DEP. CAR, 51 +/-5%, 1/4W	414540	80031	CR251-4-5P51E	2		
R16	RES, DEP. CAR, 10K +/-5%, 1/4W	348839	80031	CR251-4-5P10K	REF		
R17	RES, DEP. CAR, 510 +/-5%, 1/4W	441600	80031	CR251-4-5P510E	4		
R18	RES, DEP. CAR, 510 +/-5%, 1/4W	441600	80031	CR251-4-5P510E	REF		
R19	RES, DEP. CAR, 180K +/-5%, 1/4W	348946	80031	CR251-4-5P180K	REF		
R20	RES, DEP. CAR, 510 +/-5%, 1/4W	441600	80031	CR251-4-5P510E	REF		
R21	RES, DEP. CAR, 100 +/-5%, 1/4W	348771	80031	CR251-4-5P100E	2		
R22	RES, DEP. CAR, 220K +/-5%, 1/4W	348953	80031	CR251-4-5P220K	1		
R23	RES, VAR, 20K +/-10%, 1/2W	291609	11236	360S2034	1	1	
R24	RES, DEP. CAR, 100 +/-5%, 1/4W	348771	80031	CR251-4-5P100E	REF		
R25	RES, DEP. CAR, 51 +/-5%, 1/4W	414540	80031	CR251-4-5P51E	REF		
R26	RES, DEP. CAR, 47K +/-5%, 1/4W	348896	80031	CR251-4-5P47K	1		
R27	RES, DEP. CAR, 6.2K +/-5%, 1/4W	442368	80031	CR251-4-5P6K2	3		
R28	RES, DEP. CAR, 6.2K +/-5%, 1/4W	442368	80031	CR251-4-5P6K2	REF		
R29	RES, DEP. CAR, 6.2K +/-5%, 1/4W	442368	80031	CR251-4-5P6K2	REF		
R30	RES, DEP. CAR, 510 +/-5%, 1/4W	441600	80031	CR251-4-5P510E	REF		
RN1	RES, NETWORK, 10K +/-5%, 1/4W	364000	89536	364000	1	1	
U1	IC, LIN, OP-AMP, QUAD, COMPENSATED	402669	12040	LM324N	1	1	
U2	IC, HI-SPEED DIVIDER, 600 MHZ	428631	03797	SP8635B	1	1	
U3	IC, DUAL TYPE D, MSTR-SLAVE F/F	454959	04713	MC10131P	1	1	
U4	IC, TTL, LO-PWR, SCHOTTKY, TRI-ST	429902	12040	DM81LS95N	1	1	
U5	IC, LIN, QUAD COMPARATOR, 14-PIN DIP	387233	12040	LM339N	1	1	
U6	IC, DIG, PERIPHERAL DRIVER, 8-PIN DIP	393959	12040	DS75451AN	1	1	
U7	500 MHZ, PREAMP (TO J11)	476820	89536	476820	1		
W1	CABLE, COAX, 3 1/2 INCH	398461	89536	398461	1		
XF1	SOCKET, FUSE	403642	00779	50863-8	4		
XF2	SOCKET, FUSE	403642	00779	50863-8	REF		
XU2	SOCKET, IC, 16-PIN	276535	91506	316-AG39D	1		

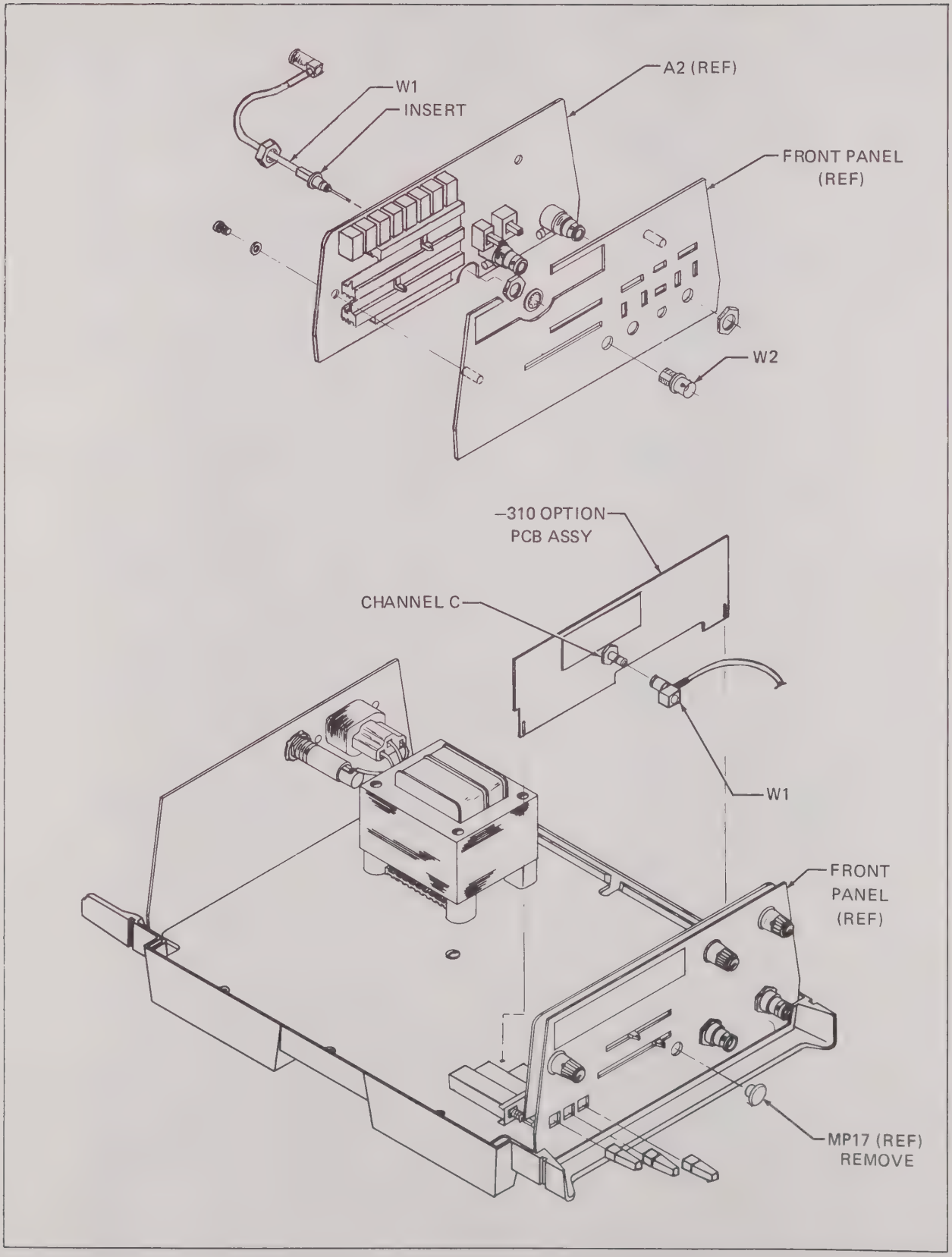


Figure 6310-5. Direct Channel C Assembly, 520 MHz

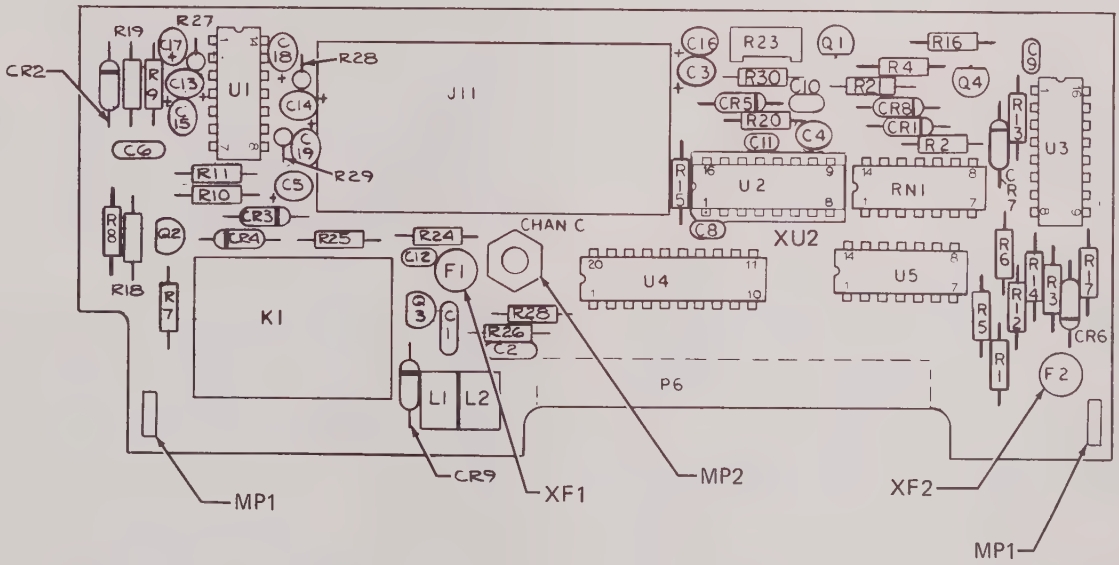


Figure 6310-5. Direct Channel C Assembly, 520 MHz (cont)

Option 72XXA-331
1300 MHz Prescaler

6331-1. INTRODUCTION

6331-2. The 72XXA-331 Option is a prescaler which extends the frequency range of the Fluke 7260A and 7261A counters to 1300 MHz. This prescaler operates from 100 MHz to 1300 MHz and has a sensitivity of 10 mV rms at 1000 MHz. Once installed, Channel C (CH C) becomes the front panel input for this option.

6331-3. As shown in Figure 6331-1, the option consists of one plug-in circuit board module (two printed circuit boards mated) and a front panel BNC jack with connecting cable. The -331 Option may be installed either at the factory or at a Fluke Service Center; however, it is not field installable. When ordering, use the option model number 72XXA-331.

6331-4. SPECIFICATIONS

6331-5. Specifications for the 1300 MHz Prescaler are listed in Table 6331-1.

6331-6. OPERATING INSTRUCTIONS

CAUTION

Keep Channel C input voltage levels below 5V rms to ensure proper operation. The prescaler is fuse-protected to prevent damage from signals above the safe operating range.

6331-7. To use the 1300 MHz Prescaler option, set the counter FUNCTION control to FREQ C and apply a signal to the CH C (Channel C) connector. All CHANNEL A and CHANNEL B controls and jacks are entirely disabled when in the Freq C mode and have no effect on the Channel C operation. The T.I. HOLDOFF (Time Interval Holdoff) is also disabled.

NOTE

Slower measurements will be encountered with the prescaler option. The option requires each RESOLUTION setting to have a 16-fold longer gate time in Channel C mode, as noted in the specifications.

6331-8. In the 0.1 Hz and 1 Hz RESOLUTION settings, the display may overflow--the OVFL LED will come on and the uppermost digits will be truncated at the left. The digits that are displayed will continue to accurately show the lower-order digits of the measurement.

6331-9. The TRIG/CONT (triggered/continuous) MODE switch on the rear panel of the main counter allows the measurement to be initiated either for signal bursts or for steady-state signals.

6331-10. Continuous Mode Operation

6331-11. Set the rear panel switch to CONT for measuring steady-state signals. Measurements will be taken consecutively, one after another, as long as the input signal is above the squelch threshold (about 3 to 5 mV). Bringing the signal from below to above threshold will reset any measurement in progress and initiate a new measurement sequence. Of course, the RESET Button will also initiate a measurement.

6331-12. Triggered Mode Operation

6331-13. Set the rear panel switch to TRIG for measuring bursts. A measurement will trigger only at the start of a burst--when the peak-envelope of the input signal crosses above the operating threshold. It will make one measurement for each burst. In order to be measured, the burst must be present longer than the gate time (specified by the RESOLUTION setting) plus approximately 2 ms.

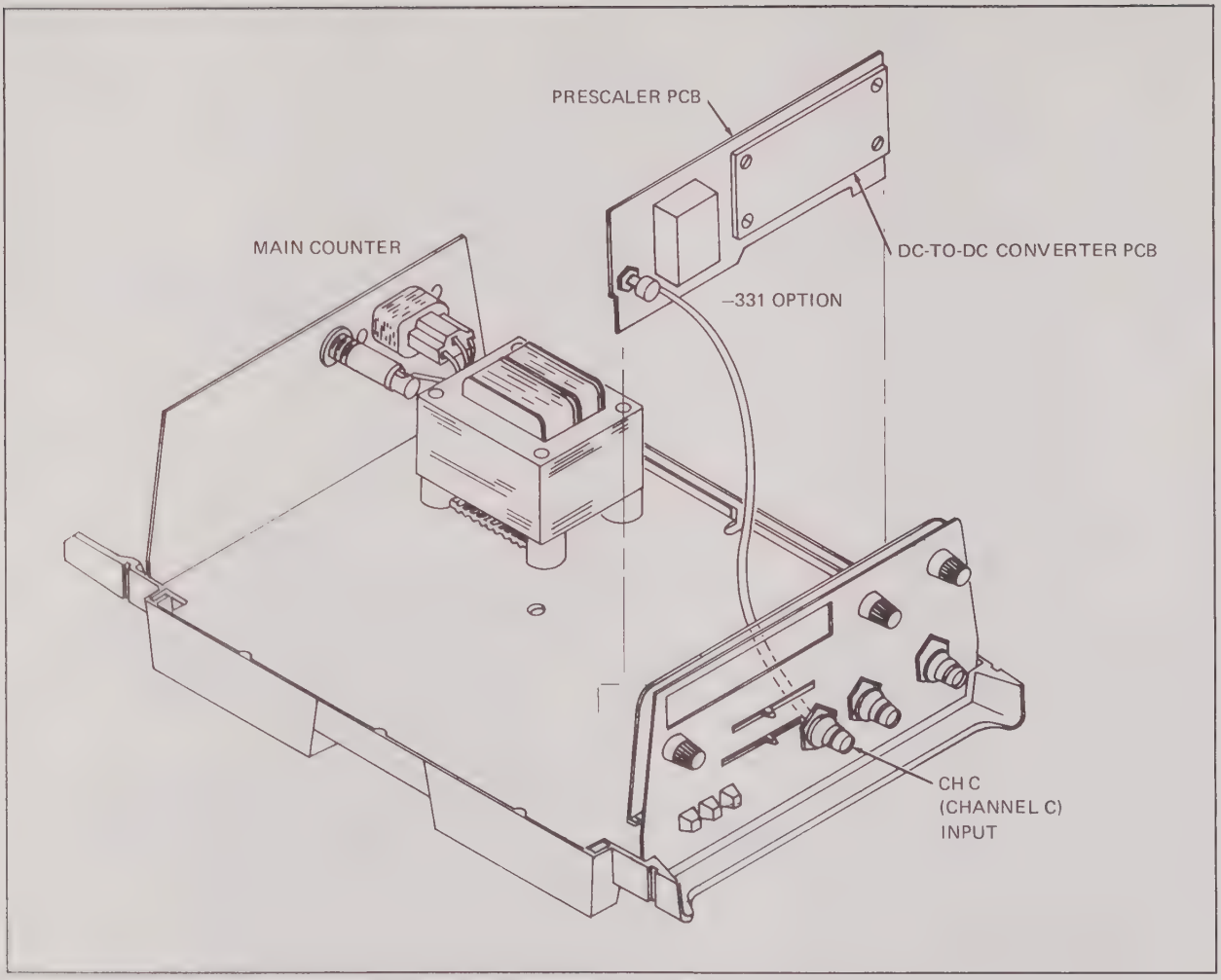


Figure 6331-1. Exploded Illustration of -331 Option and Main Counter

Table 6331-1. Specifications

RANGE:	100 MHz - 1300 MHz
SENSITIVITY:	5 mV rms, up to 600 MHz
	10 mV rms, up to 1000 MHz
	40 mV rms, up to 1300 MHz
IMPUT IMPEDANCE:	50 ohms, nominal
VSWR:	2.5 : 1, typical
MAXIMUM INPUT:	5V rms, fused
GATE TIME:	1.6 ms at 10 kHz resolution
	16 ms at 1 kHz resolution
	160 ms at 100 Hz resolution
	1.6 s at 10 Hz resolution
	16 s at 1 Hz resolution
	160 s at 0.1 Hz resolution
DISPLAY ACCURACY:	±1 count plus time base errors

6331-14. THEORY OF OPERATION

6331-15. Overall Description

6331-16. The main purpose of the -331 prescaler is to scale down the frequency of an input signal to a range acceptable by the main frequency counter. In Figure 6331-2, this operation is accomplished in the two blocks labeled Signal Divider. The effect is that higher frequencies can be measured than would otherwise be possible. The scale factor of the -331 Option is 16--that is, an input signal of 1300 MHz is scaled down to 1300/16 = 81.25 MHz. On board this option is a dc-to-dc converter which produces the –1.8 volt dc supply necessary for the frequency divider chip. A switching regulator is used rather than a linear or resistive regulator to reduce the –12 volts to –1.8 volts, because it provides the efficiency needed.

6331-17. The -331 Prescaler Option performs two other necessary functions: 1) it provides gain, since the option

replaces the front section of your main counter, and 2) it automatically lengthens by 16-fold the time the counter's main gate is open (more about this later).

6331-18. Detailed Description

6331-19. The following descriptions refer to the block diagram, Figure 6331-2, and the detailed schematics of both printed circuit boards that are included in Section 8 of this manual.

6331-20. INPUT AMPLIFIER AND SIGNAL DIVIDERS

6331-21. As shown in the block diagram, Figure 6331-2, the Channel C input signal enters through an input protection fuse, F1. Diode clamping within the hybrid circuit provides further protection from excessive input voltages. A 1300 MHz hybrid amplifier, contained in U3, then amplifies the signal. This hybrid amplifier has four stages which provide approximately 40 dB of overall gain.

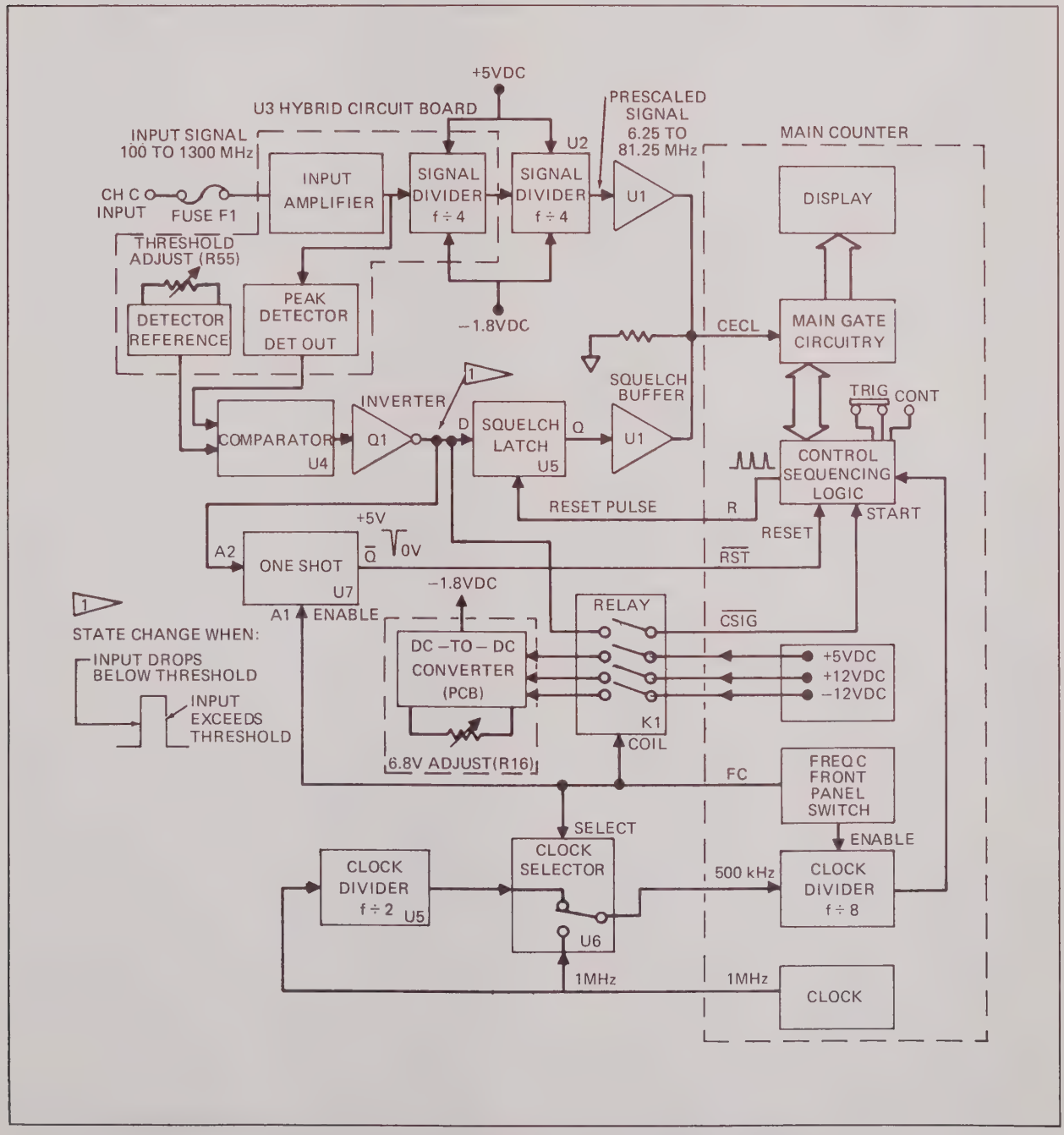


Figure 6331-2. Block Diagram of -331 Prescaler Option

6331-22. The amplifier output feeds both a divide-by-four high frequency divider and a peak detector whose output operates the squelch latch. The divider output is ac-coupled via C1 to the second divide-by-four stage, U2, for a total division of 16. As the block diagram shows, the first divide-by-four integrated circuit (IC) is included on the hybrid circuit U3, and the second is off the hybrid board. The output of U2, the prescaled signal, then passes on to a differential buffer U1 whose output (CECL) enters the main gate of the counter for subsequent accumulation and display.

6331-23. THRESHOLD AND SQUELCH CIRCUIT

6331-24. The peak detector mentioned previously is used in a squelch scheme to prevent the counter from displaying erroneous readings when no signal is applied. (The first divide-by-four is actually a locked oscillator which will free run in the absence of a signal, and be read by the counter if not squelched.) The detector output (DET OUT) is compared to a detector reference (DET REF) by comparator U4. The level of the detector reference determines the squelch threshold, and can be adjusted (Threshold Adjust, R55).

6331-25. The squelch circuit consists of the following chain of blocks shown in Figure 6331-2: peak detector, detector reference, comparator, inverter, squelch latch, and squelch buffer. When the Channel C input signal is low enough to cause the peak detector level to drop below the detector reference, then the comparator output (U4) switches to its negative limit, causing the Q1 output ($\overline{\text{CSIG}}$) to go high, to +5V. This condition at the output of Q1 is then sampled by U5, a D-type flip-flop, when the next reset pulse (R) occurs; this condition is stored at the Q output of U5. A +5V level at this point indicates the signal at the Channel C input is below the level set by the Threshold Adjust. This +5V level drives the squelch buffer U1 output (CECL line) high, which overrides (squelches) the prescaled signal. The output of the two U1 buffers are wired OR. (Emitter-coupled-logic, the device family of the Channel C U1 buffers, gives rise to the mnemonic CECL.)

6331-26. When the input signal rises above the threshold, U4 output goes high, and Q1 output (collector) goes low. At the next reset pulse (R), the squelch latch U5 transfers the low state to its output (Q), and on to the U1 output. This low state permits the prescaled signal to pass on into the main gate.

6331-27. TRIGGERED/CONTINUOUS OPERATION

6331-28. Use the TRIG/CONT switch, located on the rear panel, to switch between discretely triggered and continuously triggered modes. The triggered (TRIG) mode allows frequency measurements to be made of an RF burst, provided the burst remains high for at least the length of the gate pulse (given by the RESOLUTION) plus the 2 ms overhead necessary to initiate the measurement. As explained previously, $\overline{\text{CSIG}}$ goes low as the input signal crosses above the threshold. When the main counter is switched into the triggered (TRIG) mode, the counter will start a measurement in response to the negative-going edge of $\overline{\text{CSIG}}$--that is, when the input signal exceeds the threshold. In the continuous (CONT) mode, a measurment will be initiated not only by $\overline{\text{CSIG}}$, but also by the counter's normal sequencing signal, which indicates the completion of the previous measurement.

6331-29. One-shot U7 is used to generate a master reset pulse, $\overline{\text{RST}}$, for the main instrument every time an input signal crosses from below to above the threshold. This reset pulse is an overriding command which interrupts existing activities, resets the display to zero, and initiates a new measurement sequence, whether in triggered (TRIG) or continuous (CONT) operation. The one-shot is enabled only when the front panel Frequency C function is selected. The purpose of $\overline{\text{RST}}$ is as follows: in case there is a measurement cycle in progress, especially one with a long gate time of 16 or 160 seconds, it immediately re-starts the measurement, rather that letting the counter wait for the cycle to end.

6331-30. CLOCK SCALING

6331-31. Scaling down the input frequency by 16 requires that the gate time be lengthened by 16, in order to realize the same resolution that was obtained without prescaling. For example, a 160 MHz signal counted for 0.1 second will produce 16 million counts. The same input signal when scaled down by 16, to 10 MHz, with the same 0.1 second gate time, would produce only 1 million counts. Thus, to produce 16 million counts the gate must remain open for 1.6 seconds. Resolution is defined in Section 2 of this manual.

6331-32. Lengthening of the main gate time is accomplished by dividing the frequency of the clock which drives the gate circuitry. The clock frequency is divided by 16 to lengthen the main gate time by 16. This division takes place in two stages--each stage is labeled clock divider in Figure 6331-2. A divide-by-two (U5) on the Prescaler PCB, and an additional divide-by-eight in the main instrument. The block labeled clock selector is a NAND/NOR/INVERT gate, U6, which selects the 1 MHz or 500 kHz clock. The decision of when to divide the clock by 16 is provided by the FC (Frequency C) line. Setting the front panel FUNCTION switch to Frequency C forces the FC line high, which routes the clock signal through the divide-by-16 circuitry.

6331-33. CONVERSING POWER

6331-34. Relay K1 disconnects power to this option when it is not in use. The relay closes, connecting power to

this option by setting the front panel FUNCTION switch to Frequency C, which drives FC high, turning on transistor Q2, which activates the relay. Also on board this option is a highly efficient dc-to-dc converter which produces the -1.8 volt supply necessary for the signal dividers.

6331-35. DC-TO-DC CONVERTER

6331-36. The DC-to-DC Converter is designed around a pulse-width modulator (PWM) chip, U1, which is used to regulate the output to -1.8V, the dc supply required by the signal dividers. The circuit is actually designed to supply an output that is 6.8V below the +5V supply. Therefore the +5V and -1.8V supplies present a constant 6.8 volt difference to the signal divider ICs, even when battery powered, and the -5V supply falls from 5.5V to 4.5V as the batteries discharge. This regulation is necessary for the signal dividers to maintain maximum performance during battery operation. The 6.8V regulation is accomplished by referencing the voltage reference VR1 and the feedback resistive divider R15. R16, R17 to +5V.

6331-37. Refer to waveforms shown in the DC-to-DC Converter schematic. The PWM (U1) outputs (at pin 12) a rectangular waveform alternating between +5V and 0V The period (but not duty cycle) of this signal is determined by R5 and C2. This signal causes both Q1 and Q3 to alternate together between off and on, the collector of Q3 alternating between +0.7V and 12V. The PWM compares the reference voltage at pin 1 to the feedback voltage at pin 2 and adjusts the the duty cycle of Q1 and Q3, until the feedback voltage equals the reference voltage. This balance consequently fixes the output voltage.

6331-38. The inductor-current ramps linearly up and down in response to the alternating +0.7V and -12V at Q3; its average current is equal to the load current. Capacitor C6 filters the ripple on the output. Being a non-dissipating component, L1 helps maintain high efficiency. Transistors Q1 and Q3 switch continually, between saturation and cutoff. Resistor R14 and resistor Q2 form current limiting protection when the current through R14 exceeds approximately 150 mA. When this happens, Q2 forces sensing pin 5 to -12V, which shuts down U1 Resistor R8 and capacitor C7 limit the open-loop gain and provide compensation of the amplifier located inside U1.

6331-39. MAINTENANCE

6331-40. Fuse Replacement

6331-41. The Channel C input to the -331 Option is overvoltage protected by a series fuse F1. The fuse will blow before the input exceeds a level safe for the circuit components, about 10V rms.

NOTE

A spare fuse is located on the circuit board.

6331-42. Figure 6331-3 shows the locations of both the in-circuit fuse and spare fuse. Fuse replacement requires removal of the top cover from the chassis; refer to Disassembly near the beginning of Section 4 of this manual. Be especially careful when following that procedure to prevent damage to the internal circuits. As shown in Figure 6331-3, the in-circuit fuse is located on the circuit board just next to the input cable. It is approximately ¼ inch in height and diameter, and has a clear plastic cap. Unplug the fuse and test for continuity with an ohmmeter. If open, replace it with the spare fuse located elsewhere on the same circuit board. To order another fuse, contact your nearest Fluke Service Center, found listed in Section 7, and order Fluke Part Number 370577 (Littlefuse Part Number 273.200).

6331-43. Performance Test

6331-44. Use the following tests to check the performance and to verify the specifications of the 1300 MHz Prescaler Option.

Set-up Procedure:

1. Table 6331-2 lists the required test equipment (The step attenuator is necessary because the generator's built-in attenuator produces an increasingly worse signal-to-noise ratio at large attenuations.)

2 Connect your Fluke frequency counter that is to be tested, hereafter called UUT (Unit Under Test), to the above equipment as shown in Figure 6331-4. Disregard the DVM shown in the figure: it is used for the Calibration Adjustment procedures only.

3. Set the controls on the UUT as follows

a. Front Panel:

FUNCTION-----FREQ C
RESOLUTION---100 Hz

b. Rear Panel:

REF switch----------EXT
TRIG/CONT MODE switch-----CONT

c. Turn on the power to the UUT, and allow it to warm up for at least 30 minutes.

d. All other controls may be at any position.

4. Set the Signal Generator to an output level of +10 dBm (707 mV into 50 ohms). Leave the generator output at this level throughout the entire performance test; use the 60 dB Step Attenuator to control the level to the UUT.

6331-45. SENSITIVITY TEST

6331-46. This procedure examines the UUT measurement error at the rated sensitivity at three frequencies:

1. To start with, set the Signal Generator frequency to 100 MHz, and set the Step Attenuator at 43 dB (as listed below). The UUT should measure and display the frequency selected, within ±1 count in the lowest-order digit.

Signal Generator Frequency	Step Attenuator Setting
100 MHz	43 dB (5 mV)
600 MHz	37 dB (10 mV)
1300 MHz	25 dB (40 mV)

2. Repeat the previous step (1) at 600 MHz and 1300 MHz, using the Step Attenuator setting listed for each frequency.

6331-47. THRESHOLD ADJUSTMENT TEST

1. Set the Step Attenuator to 52 dB (UUT input level of 1.8 mV).

2. Set the Signal Generator frequency to 600 MHz. The display should read 0.0000. The display goes to zero to indicate the option is operating at a level below its rated sensitivity. Change the step attenuator setting to 45 dB. The UUT should display 600 MHz.

6331-48. TRIGGERED MODE TEST

1. Set the UUT rear panel TRIG CONT MODE switch to TRIG

2 Set the Signal Generator frequency to 800 MHz if not already there; set the Step Attenuator to 53 dB

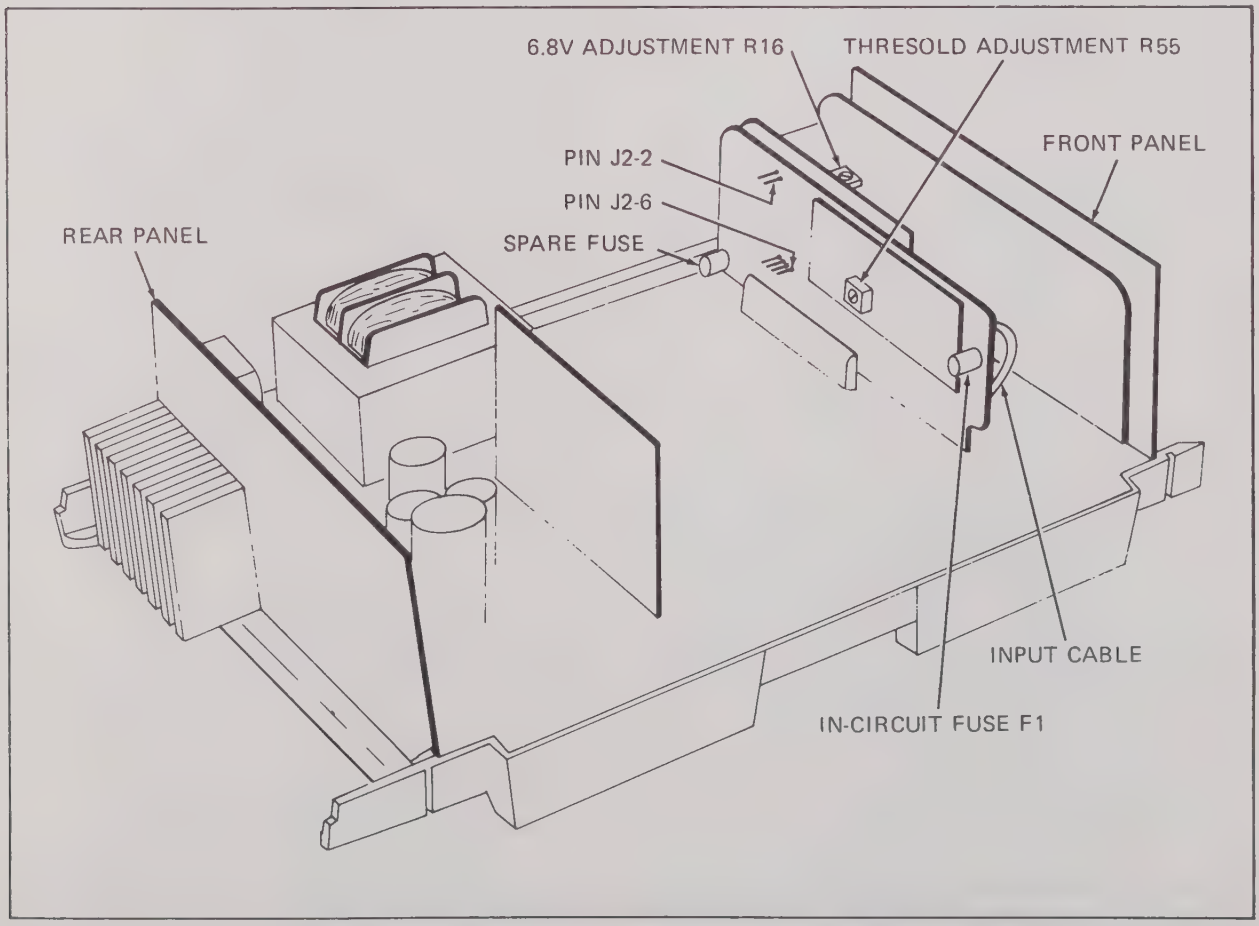


Figure 6331-3. Fuse and Adjustment Locations of -331 Option

(1.6 mV at the UUT input). At this time the counter should not be gating--the gating light should not be flashing.

3. Increase the signal level 16 dB by changing the Step Attenuator setting to 37 dB (10 mV). The counter should gate once and read 800.0000 MHz ±1 count. Using the Signal Generator's 10 MHz reference allows the counter to read this accurately.

6331-49. Calibration Adjustments

6331-50. Calibration adjustments should be performed if the -331 fails the performance test and after repairs are made to the option. The location of all adjustments is shown in Figure 6331-3.

6331-51. Calibration of the -331 Prescaler Option follows a procedure similar to, but more involved than the Performance Test. All the steps of the previous performance test are included in the following calibration adjustment procedure; once you have finished the following procedure you needn't go back and do the performance test.

6331-52. In order to perform calibration adjustments on the -331, you must remove the top cover from the

Table 6331-2. Required Test Equipment

EQUIPMENT TYPE	REQUIRED SPECIFICATIONS	RECOMMENDED TYPE
Synthesized Signal Generator	100 MHz - 1300 MHz, 10 mV	Hewlett-Packard HP8660C
60 dB Step Attenuator	1 dB step with N-female connectors	Weinschel Eng. AD117-69-33
Adapter (1)	N-male to BNC-male	Pomona 4297 (UG1034/U)
Adapters (2)	N-male to BNC-female	Tektronix 103-0045-00 (UG201A/U)
Coax Cable	50 ohm with BNC-male connectors 6" long	RG58A/U
Coax Cable	50 ohm with BNC-male connectors	Fluke Y9111 RG58C/U

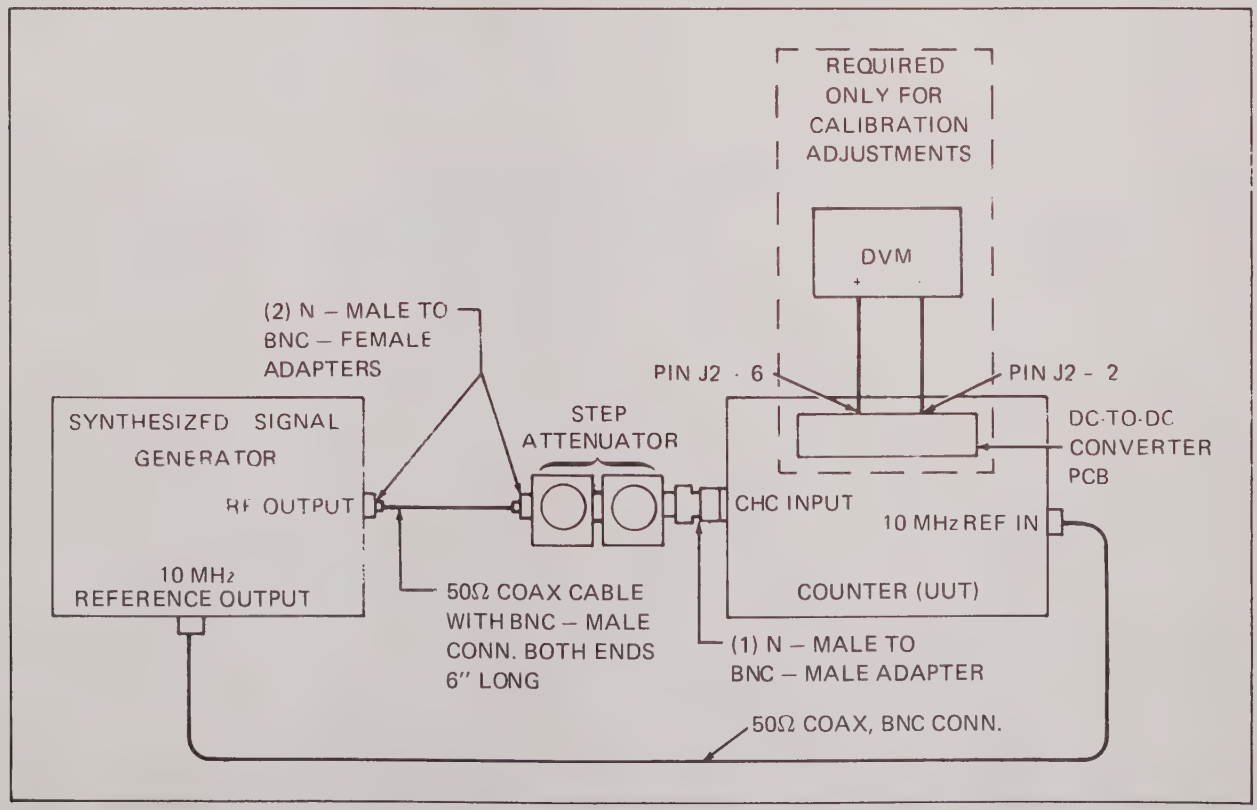

REQUIRED ONLY FOR CALIBRATION ADJUSTMENTS
DVM
(2) N – MALE TO BNC – FEMALE ADAPTERS
PIN J2 - 6
PIN J2 - 2
SYNTHESIZED SIGNAL GENERATOR
STEP ATTENUATOR
DC-TO-DC CONVERTER PCB
RF OUTPUT
CHC INPUT
10 MHz REF IN
10 MHz REFERENCE OUTPUT
50Ω COAX CABLE WITH BNC – MALE CONN. BOTH ENDS 6" LONG
COUNTER (UUT)
(1) N – MALE TO BNC – MALE ADAPTER
50Ω COAX, BNC CONN.

Figure 6331-4. Equipment Connections for Testing -331 Option

counter under test. It is important for you to follow the steps below in the order given.

6331-53. SET-UP PROCEDURE

1. Remove the top cover as described in the Disassembly procedure in Section 4 of the Fluke counter manual. Follow that procedure very carefully to prevent damage to the internal circuits.

2. Perform all four steps of the Set-up Procedure listed in the Performance Test previously described. In addition to the equipment listed, set up the Digital Voltmeter (DVM) shown in Figure 6331-4.

6331-54 6.8V SUPPLY DIFFERENCE

6331-55 This procedure adjusts R16 for a DC-to-DC Converter output (-1.8V) that is 6.8 volts below the +5V supply

1. As illustrated in Figure 6331-4, connect the DVM (+) lead to pin J2-6 of the DC-to-DC Converter PCB, and the DVM (-) lead to pin J2-2

2 Turn the UUT on and let it warm up for 30 minutes

3 Adjust R16 for a DVM reading between 6.78 and 6.82 volts if it is outside this range

4 Disconnect the DVM

6331-56. VERIFY THE UUT SENSITIVITY (WITH THRESHOLD OFF)

1 Find R55, the Threshold Adjust trimpot, located as shown in Figure 6331-3. Turn R55 fully counterclockwise (when looking at the trimpot); this turns the threshold off. Now that the threshold is off, the UUT will continue to display readings, even with no input.

2. Set the Signal Generator to 100 MHz, +10 dBm

3. Set the Step Attenuator to 30 dB to produce a 22.4 mV level to the UUT. The UUT should now be gating (the GATE light flashing), and the display should read 100.0000 MHz plus or minus 1 count in the lowest-order digit.

4. Increase the attenuation (decrease the level) in 1 dB steps until the display has more than ±1 count error. Back off 1 dB (that is, to within ±1 count) and record the attenuator setting. The UUT sensitivity is within specifications if the Step Attenuator reads greater than what is listed in Table 6331-3 for the frequency tested

5 Repeat the previous step at every multiple of 100 MHz, using the acceptance data listed in Table 6331-3.

Table 6331-3. Calibration Sensitivity

SIGNAL GENERATOR FREQUENCY MHz	SENSITIVITY ACCEPTABLE IF STEP ATTENUATOR SETTING IS GREATER THAN:
100 200 300 400 500	43 dB (less than 5 mV)
600 700 800 900 1000	37 dB (less than 10 mV)
1100 1200 1300	25 dB (less than 40 mV)

6331-57. THRESHOLD ADJUSTMENT

6331-58. The Threshold Adjust trimpot (R55) determines the input level below which the counter stops taking measurements, and instead displays zero.

1. Set the Step Attenuator to 49 dB (UUT input level of 2.5 mV); set the Generator Frequency at 600 MHz.

2. Rotate the Threshold Adjust trimpot (R55), located in Figure 6331-3, to the point where the display drops to a 0.0000 reading. The threshold is now properly adjusted.

6331-59. TEST THE TRIG MODE

6331-60. This is only a test and has no adjustment associated with it.

1. Set the UUT rear panel TRIG/CONT MODE switch to TRIG.

2. Set the Signal Generator frequency to 800 MHz if not already there. Set the Step Attenuator to 53 dB (1.6 mV at the UUT input).

3. At this time the counter should not be gating--the gating light should be off. Change the Step Attenuator setting to 37 dB (10 mV). The counter should gate once and read 800.0000 MHz $\pm$1 count if the trigger circuit works properly.

6331-61. LIST OF REPLACEABLE PARTS

6331-62. A list of replaceable parts for the 72XXA-331 Option is given in Table 6331-4, 6331-5, and 6331-6. Refer to Section 5 of this manual for ordering information.

6331-63. There are two printed circuit boards in the -331 Option. They are shown together in the Final Assembly Figure 6331-5, as well as separately, in Figures 6331-6 and 6331-7.

Table 6331-4. Final Assembly, 1300MHz Prescaler

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	NOTE
	FINAL ASSEMBLY, 1300 MHZ PRESCALER FIGURE 6331-5 (72XXA-331K)	ORDER	BY	OPTION 72XXA-331K			
A1	1300 MHZ PRESCALER PCB ASSEMBLY	475913	89536	475913	1		
A2	DC TO DC CONVERTER PCB ASSEMBLY	475889	89536	475889	1		
H1	LOCKWASHER, #6	110338	89536	110338	4		
H2	SCREW, PHP, 6-32 X 1/4	152140	89536	152140	4		
KIT	RECOMMENDED SPARE PARTS KIT (72XXA-331)	541490	89536	541490	AR		
TM1	INSTRUCTION SHEET 72XXA-331K (NOT SHOWN)	546087	89536	546087	1		*
W1	COAX CABLE ASSEMBLY	521724	89536	521724	1		

* FOR KIT INSTALLATION

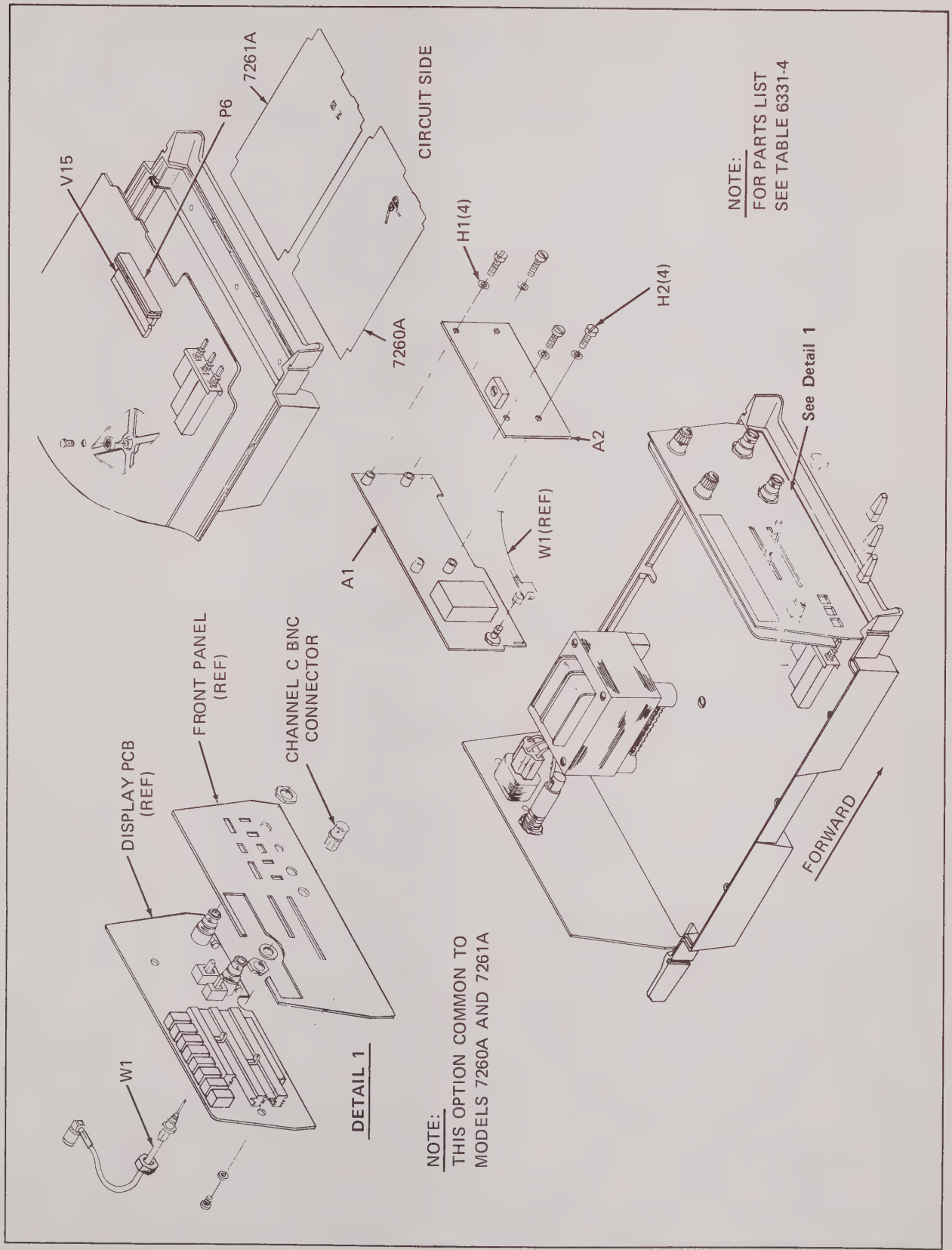


Figure 6331-5. Final Assembly, 1300 MHz Prescaler

Table 6331-5. 1300MHz Prescaler PCB Assembly

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG. PART NO.	TOT QTY	REC QTY	NOTE
A1	1300 MHZ PRESCALER PCB ASSEMBLY FIGURE 6331-6 (7260A-4004T)	475913	89536	475913	REF		
C1	CAP, CER, 0.01 UF +/-20%, 100V	407361	72982	8121-A100-W5R-103M	5		
C2	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	6		
C3	CAP, CER, 0.01 UF +/-20%, 100V	407361	72982	8121-A100-W5R-103M	REF		
C4	CAP, CER, 0.01 UF +/-20%, 100V	407361	72982	8121-A100-W5R-103M	REF		
C5	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C6	CAP, CER, 0.01 UF +/-20%, 100V	407361	72982	8121-A100-W5R-103M	REF		
C7	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C8	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C9	CAP, CER, .001 UF +/-20%, 500V	402966	72982	8121-A100-W5R-102M	2		
C10	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C11	CAP, CER, 0.01 UF +/-20%, 100V	407361	72982	8121-A100-W5R-103M	REF		
C12	CAP, CER, .001 UF +/-20%, 500V	402966	72982	8121-A100-W5R-102M	REF		
C13	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
CR1	DIODE, SI, HI-SPEED SWITCHING	203323	07910	1N4448	2		
CR2	DIODE, GE, 80 MA, 100 PIV	149187	93332	1N270	1		
CR3	DIODE, SI, HI-SPEED SWITCHING	203323	07910	1N4448	REF		
F1	FUSE, 1/5 AMP (AND 1 SPARE)	370577	75915	273.200	2	5	
H1	SPACER (NOT SHOWN)	446351	89536	44631	4		
J1	SOCKET, BNC CONNECTOR	352450	98291	51-051-0000	1		
J2	CONNECTOR, POST (NOT SHOWN)	267633	00779	86144-1	6		
K1	RELAY, DRY REED	494732	21317	E54AX5	1		
L1	CHOKE, 6-TURN	320911	89536	320911	2		
L2	CHOKE, 6-TURN	320911	89536	320911	REF		
P3	CONNECTOR, RECEPTACLE	375329	00779	85863-3	2		
P4	CONNECTOR, RECEPTACLE	375329	00779	85863-3	REF		
Q1	XSTR, SI, NPN	218396	04713	2N3904	1	1	
Q2	XSTR, SI, NPN	381798	04713	MPSA-13	1	1	
R1	RES, DEP. CAR, 100 +/-5%, 1/4W	348771	80031	CR251-4-5P100E	3		
R2	RES, DEP. CAR, 100 +/-5%, 1/4W	348771	80031	CR251-4-5P100E	REF		
R7	RES, DEP. CAR, 100 +/-5%, 1/4W	348771	80031	CR251-4-5P100E	REF		
R8	RES, DEP. CAR, 10K +/-5%, 1/4W	348839	80031	CR251-4-5P10K	2		
R9	RES, DEP. CAR, 100K +/-5%, 1/4W	348920	80031	CR251-4-5P100K	1		
R10	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-4-5P4K7	2		
R12	RES, DEP. CAR, 10K +/-5%, 1/4W	348839	80031	CR251-4-5P10K	REF		
R13	RES, DEP. CAR, 47K +/-5%, 1/4W	348896	80031	CR251-4-5P47K	1		
R14	RES, DEP. CAR, 220K +/-1%, 1/4W	348953	80031	CR251-4-5P220K	1		
R15	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-4-5P4K7	REF		
U1	IC, TRIPLE LINE RECEIVER, 16-PIN DIP	369702	18324	N10116B	1	1	
U2	IC, ECL, 1600 SERIES, GHZ PRESCALER	472787	04713	MC1697P	1	1	
U3	IC, HYBRID, 1300 MHZ	490664	89536	490664	1	1	
U4	IC, LIN, OP-AMP, LO BIAS CURRENT	413732	12040	LM308N	1	1	
U5	IC, TTL, DUAL, "D" TYPE CLEAR AND PRESET	393124	01295	SN74L574N	1	1	
U6	IC, TTL, QUAD, 2-INPUT, POS, NAND GATE	393033	01295	SN74LS00N	1	1	
U7	IC, MONOSTABLE, MULTIVIBRATOR	293050	01295	SN74121N	1	1	
XF1	SOCKET, FUSE	403642	00779	50863-8	4		
XU3	SOCKET, IC, (U3)	376418	22526	75060-007	23		
Z1	RESISTOR NETWORK, 510 +/-2%, 1/8W	459974	89536	459974	1		

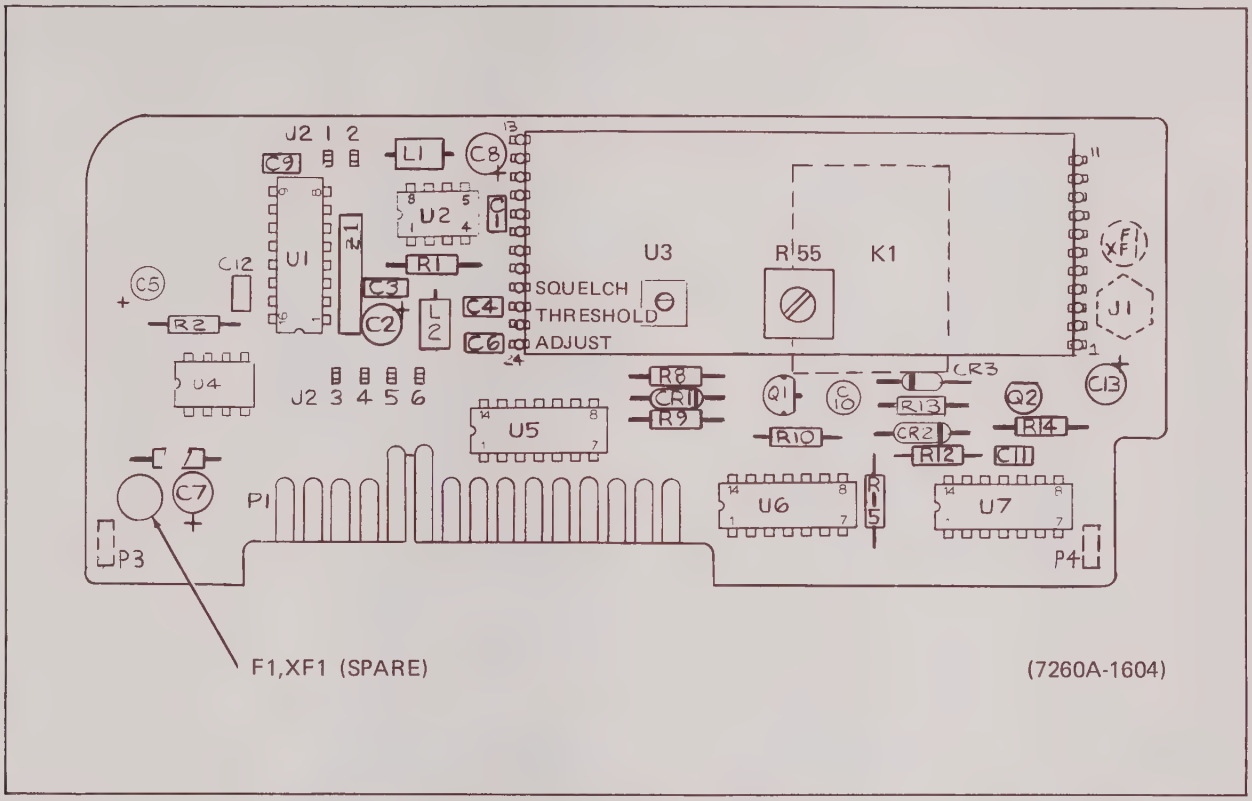
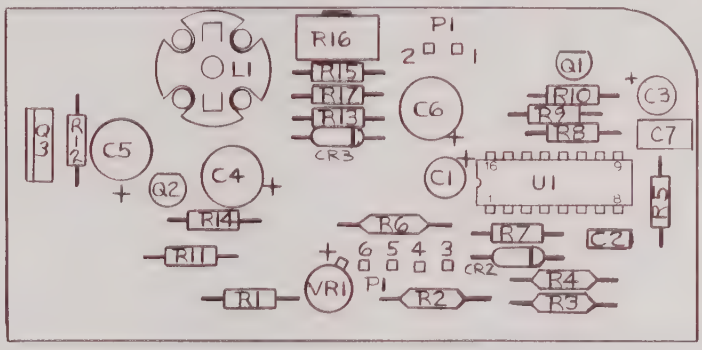


Figure 6331-6. A1 1300 MHz Prescaler PCB Assembly

Table 6331-6. DC-to-DC Converter PCB Assembly

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	NOTE
A2	DC-TO-DC CONVERTER PCB ASSEMBLY FIGURE 6331-7 (7260A-4005T)	475889	89536	475889	REF		
C1	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	2		
C2	CAP, CER, 1000 PF +/-20%, 500V	402966	32897	8121-A100-W5R-102M	1		
C3	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C4	CAP, TA, 150 UF +/-20%, 20V	422576	56289	196D157X0020TA1	1		
C5	CAP, TA, 150 UF +/-20%, 20V	422576	56289	196D157X0020TA1	REF		
C6	CAP, TA, 220 UF +/-20%, 6V	408682	56289	196D227X0006TE4	1		
C7	CAP, CER, 0.22 UF +/-20%, 50V	309849	71590	CW30C224K	1		
CR2	DIODE, SI, HI-SPEED SWITCHING	203323	07910	1N4448	1		
CR3	RECTIFIER, SI, FAST RECOVERY, 100V	495739	14099	3FF10	1		
L1	INDUCTOR	521500	89536	521500	1		
MP1	INSULATOR, XSTR, (TO VR1) (NOT SHOWN)	175125	07047	10172-DAP	1		
P1	CONNECTOR, RECEPTACLE	267476	00779	85861-2	6		
Q1	XSTR, SI, PNP	195974	04713	2N3906	1		
Q2	XSTR, SI, NPN	218396	04713	2N3904	1		
Q3	XSTR, SI, NPN	325761	09214	D44C5	1		
R1	RES, DEP. CAR, 2K +/-5%, 1/4W	441469	80031	CR251-4-5P2K	2		
R2	RES, MTL. FILM, 130K +/-1%, 1/8W	221648	91637	MFF1-81303F	2		
R3	RES, MTL. FILM, 249K +/-1%, 1/8W	268805	91637	CMF552493F	2		
R4	RES, MTL. FILM, 249K +/-1%, 1/8W	268805	91637	CMF552493F	REF		
R5	RES, DEP. CAR, 12K +/-5%, 1/4W	348847	80031	CR251-4-5P12K	1		
R6	RES, MTL. FILM, 130K +/-1%, 1/8W	221648	91637	MFF1-81303F	REF		
R7	RES, DEP. CAR, 1.5K +/-5%, 1/4W	343418	80031	CR251-4-5P1K5	1		
R8	RES, DEP. CAR, 1M +/-5%, 1/4W	348987	80031	CR251-4-5P1M	1		
R9	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	2		
R10	RES, DEP. CAR, 2K +/-5%, 1/4W	441469	80031	CR251-4-5P2K	REF		
R11	RES, DEP. CAR, 3.9K +/-5%, 1/4W	342600	80031	CR251-4-5P3K9	1		
R12	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	REF		
R13	RES, DEP. CAR, 1.8K +/-5%, 1/4W	441444	80031	CR251-4-5P1K8	1		
R14	RES, DEP. CAR, 4.7 +/-2%, 1/4W	342683	80031	CR251-2-5P4.7E	1		
R15	RES, DEP. CAR, 5.6K +/-5%, 1/4W	442350	80031	CR251-4-5P5K6	1		
R16	RES, VAR, CERMET, 200 +/-10%, 1/2W	285148	11236	360S206A	1		
R17	RES, DEP. CAR, 1.1K +/-5%, 1/4W	348797	80031	CR251-4-5P1K1	1		
U1	IC, LIN, REG PULSE WIDTH MODULATOR	454678	01295	SG3524N	1		
VR1	IC, LIN, LOW VOLTAGE REFERENCE 1.22V	452771	89536	452771	1		



(7260A-1605)

Figure 6331-7. DC-to-DC Converter PCB Assembly

Option -521
Printer Interface

521-1. INTRODUCTION

521-2. The purpose of the Printer Interface is to allow a Fluke counter (7220A, 7250A, 7260A, or 7261A) to be connected to a Fluke printer (2020A, 2021A, or 2030A) for printed output of counter measurements. The Printer Interface consists of the 72XXA-521 Digital Interface PCB, which is factory-installed in the counter.

NOTE

The 72XXA-521 Digital Interface PCB is also used in the IEEE Interface system for the counters. For information about its function in the IEEE Interface, refer to the 72XXA-521/-522 IEEE Interface.

521-3. The 2020A or 2021A printers must have Printer Optioin -004 installed. The 2030A is ready for connection without any additional options. The counter and printer are connected by an accessory cable. The cable is available in either a 2 foot (Y7203), or 5 foot (Y7204) length.

521-4. Data is transferred from the counter to the printer in a bit-parallel, character-serial manner. The printout from the printer includes the measurement reading of the counter and the measurement unit.

521-5. OPERATING INSTRUCTIONS

521-6. Preparation

521-7. To prepare the instruments for printing measurements, follow these steps:

1. Connect the counter and printer together via cable Y7203 or Y7204. Cable connections are made at the rear panel of each instrument.

2. Apply power to each instrument.

3. Apply a valid input signal to the counter, and set the controls as desired.

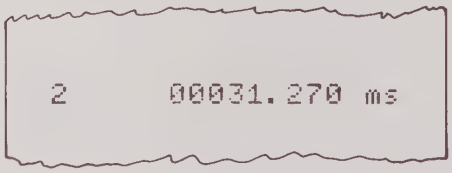
4. Set the printer controls as desired. If necessary, refer to the printer manual for operating instructions.

521-8. Printing Measurements

521-9. Figure 521-1 shows three examples of measurement printouts made by a 2030A printer. Notice in all 3 examples that all counter digits are printed (either 8 or 9, depending on the counter) including any leading zeros. Notice also in the first example that 8 digits are printed for the 7250A. The 7250A has a 7 digit display, but it supplies 8 digits of valid information to the printer.

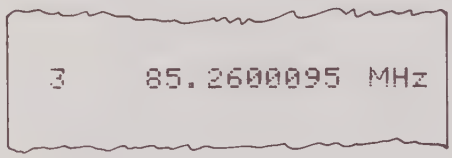
521-10. The numbers 2 and 3 in the column at the far left are non-selectable instrument addresses which have been preassigned at the factory in conformance with a printer addressing feature. All the counters have been assigned address 2 except the 7220A, which has been assigned address 3. The 7220A has a unique address because its measurement capacity is one digit greater than the other counters.

521-11. The addresses correspond to a jumper pin on the Digital Interface PCB in the counter. If the printer does not print measurement data correctly, or if it does not print at all, the jumper may be in the wrong position. To check the position or move the jumper, refer to the following paragraph.



Period Measurement made by 7250A in PER A mode with 1 μs resolution.

Frequency measurement made by 7260A in FREQ A mode with 1 Hz resolution.



Frequency measurement made by 7220A in FREQ A mode with .1 Hz resolution.

Figure 521-1. Printer Output Examples.

521-12. Moving the Address Jumper

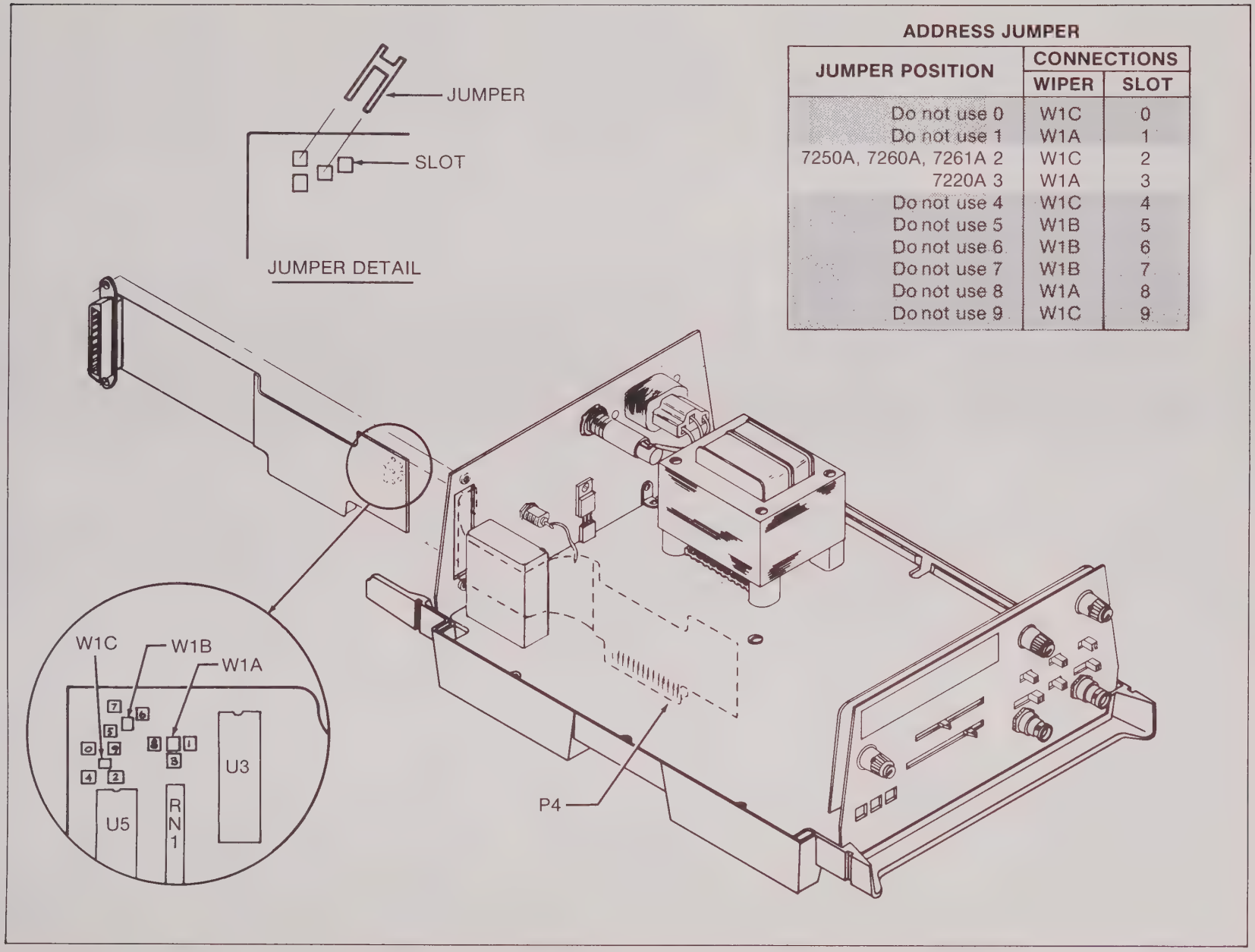
WARNING

THESE SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID ELECTRIC SHOCK, DO NOT PERFORM ANY SERVICING UNLESS YOU ARE QUALIFIED TO DO SO.

521-13. To examine the address jumper, disconnect the counter power cord and remove the top cover of the counter. Be careful not to separate the front and rear panels from the bottom case half. Locate the jumper on the upper left corner of the component side of the Digital Interface PCB. Refer to the table in Figure 521-2, and examine the jumper to determine the address selected. If the proper address is not selected, remove the jumper pin by pulling it straight out. Refer to the table in Figure 521-2 and determine the proper wiper and slot location (the jumper slot numbers are also printed on the back of the PCB). Firmly insert the jumper into place.

521-14. Operating Notes

521-15. In the single print mode, the printer prints the first counter reading it receives and then stops. In the continuous print mode, the printer prints out counter readings as it receives them, up to a maximum rate of 3 readings per second. When the measurement cycle rate of the counter is greater than 3 per second (such as frequency measurements made with 100 Hz resolution), then not all counter readings will be printed out. The printer also will not print out readings made in the Totalize mode by the 7250A, 7260A, or 7261A.



ADDRESS JUMPER

JUMPER POSITION	CONNECTIONS	
	WIPER	SLOT
Do not use 0	W1C	0
Do not use 1	W1A	1
7250A, 7260A, 7261A 2	W1C	2
7220A 3	W1A	3
Do not use 4	W1C	4
Do not use 5	W1B	5
Do not use 6	W1B	6
Do not use 7	W1B	7
Do not use 8	W1A	8
Do not use 9	W1C	9

Figure 521-2 Address Jumper

521-16. It is important to note that the printer gives no indication when an overflow condition exists in the counter. The printer will print whatever digits are present on the display at the end of the reading, whether the counter display has overflowed or not. The one exception to this is the 7250A, which supplies eight digits of valid information to the printer before overflowing, even though it has a seven digit display.

521-17. THEORY OF OPERATION

521-18. Overview

521-19. An overview of the operation of the Printer Interface is presented at the top of Figure 521-3. As shown in the figure, the printer functions primarily as a passive listener which receives and prints counter readings without affecting the operation of the counter. The printer does have a limited talk function, however. It must first send an address to the Printer Interface and have the address acknowledged by the Interface before data can be transferred from the counter.

521-20. An expanded view of the interface operation is shown in the large box at the bottom of Figure 521-3. Data transfer is controlled by the control logic, which receives address input from the printer, and three inputs from the counter, OSC, DS1, and BUSY. OSC is the oscillator signal from the scan oscillator that controls the timing of the internal strobing and mutiplexing of the counter. DS1 is the first Digit Strobe (LSD) of the counter, and BUSY is a signal from the control logic of the counter which indicates that a measurement cycle is in progress.

521-21. The Interface Control Logic has three outputs. One output enables the Data Buffer, and the other two are the control lines $\overline{\text{DATVAL}}$ and $\overline{\text{ADRVAL}}$ that are sent to the printer to enable data transfer.

521-22. Detailed Description

521-23. The following paragraphs discuss the sequence of events that take place before, during, and after data transfer. Refer to the block diagram at the bottom of Figure 521-3. The timing can be seen at the top of Figures 521-4 and 521-5, and the circuits are shown in detail in the schematic in Section 8 of the counter Instruction Manual.

521-24. ADDRESS DECODING

521-25. Data Transfer is initiated by the printer. The printer places a 4 bit BCD address on lines A0, A1, A2 and A3. The BCD address is converted to decimal, and if the address corresponds to the address selected by the address jumper, a high signal passes on to the Control Logic. This signal then enables the Data Buffer, and is also inverted and returned to the printer as a low $\overline{\text{ADRVAL}}$.

521-26. DATA TRANSFER

521-27 The low $\overline{\text{ADRVAL}}$ is sent to the microcomputer of the printer and indicates that the Printer Interface has received the address and the counter is preparing to transfer data. After the counter takes a reading, BUSY goes low, then high, which tells the Interface Control Logic a reading has been completed. The next DS1 digit strobe enables the $\overline{\text{DATVAL}}$ line, which is the inverted OSC signal. The digits of the information are now transferred in the sequence indicated in Figures 521-4 and 521-5. The 7220A is shown in a separate figure because it is a nine-digit counter, and nine digits of information are passed instead of eight.

521-28. The timing of the data transfer is controlled by the $\overline{\text{DATVAL}}$ pulses. One $\overline{\text{DATVAL}}$ pulse occurs for each digit of information transferred. All the counters have eight $\overline{\text{DATVAL}}$ pulses except the 7220A, which has nine for its nine digits. The second DS1 digit strobe disables the $\overline{\text{DATVAL}}$ pulses, thus ending the data transfer.

521-29. Data Format

521-30. The format for the data transfer is shown in Figures 521-4 and 521-5. The digits are transferred in the sequence shown, beginning with the LSD, then the MSD, and continuing in descending order of significance. Note that the 7250A provides eight digits of information to the printer even though the 7250A has a seven digit display. The MSD in Figure 521-5 is not displayed on the 7250A, but is printed by the printer. The seven digits displayed on the 7250A are 2SD-LSD.

521-31. There are six lines on which measurement data passes from the counter to the printer. Four of the lines (B1, B2, B4 and B8) transfer the measurement reading in BCD. The DP and UX lines are used to indicate when to insert the decimal point and the type of measurement unit.Table 521-1 shows an example of the format for the transmission of measurement data from a 7250A.

521-32. MAINTENANCE

521-33. Troubleshooting

521-34. If the printer does not print measurment data correctly, or if it does not print at all, first check the position of the address jumper on the Digital Interface PCB. Refer to the section on Moving the Address Jumper in the Operating Instructions.

521-35. If the printer still does not print data correctly, make sure the printer and counter are properly connected with cable Y7203 or Y7204. Apply power to the instruments, select desired settings, and apply a valid input signal to the counter. A non-burst mode must be selected for a 7220A. Use an oscilloscope and complete the procedure given in Table 521-2.

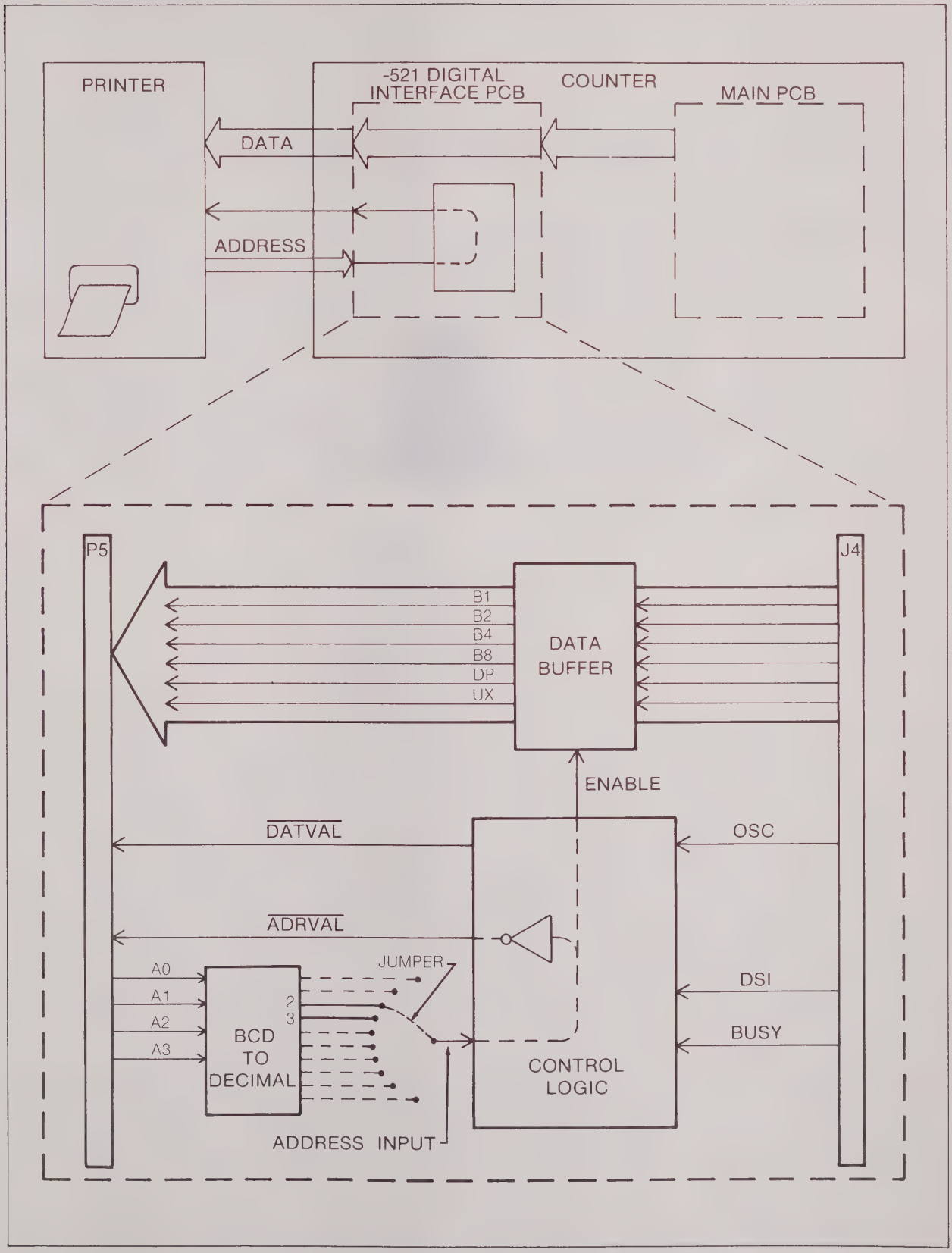


Figure 521-3 Interface Block Diagram

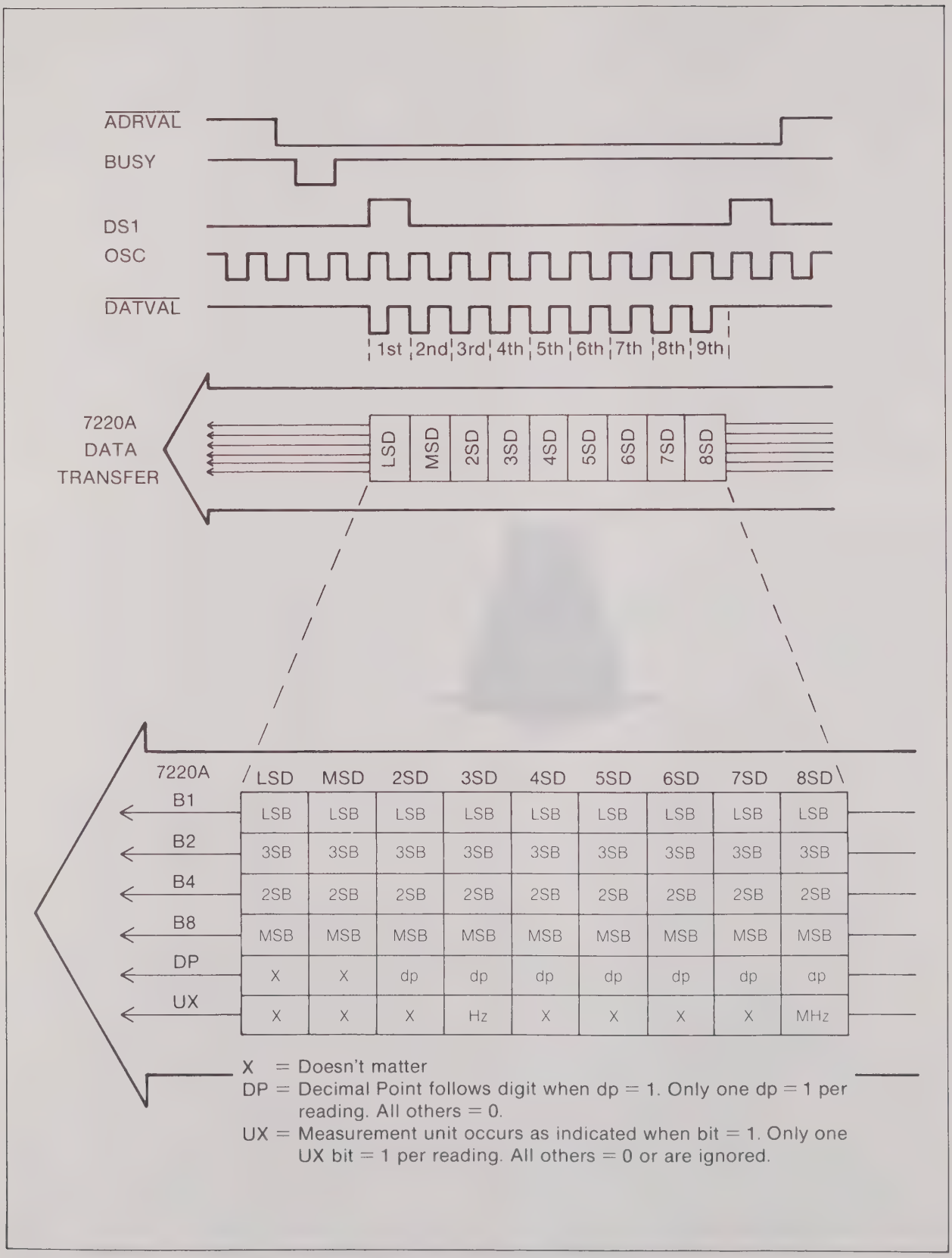

ADRVAL
BUSY
DS1
OSC
DATVAL
1st 2nd 3rd 4th 5th 6th 7th 8th 9th
7220A DATA TRANSFER
LSD MSD 2SD 3SD 4SD 5SD 6SD 7SD 8SD
7220A
LSD MSD 2SD 3SD 4SD 5SD 6SD 7SD 8SD
B1 LSB LSB LSB LSB LSB LSB LSB LSB LSB
B2 3SB 3SB 3SB 3SB 3SB 3SB 3SB 3SB 3SB
B4 2SB 2SB 2SB 2SB 2SB 2SB 2SB 2SB 2SB
B8 MSB MSB MSB MSB MSB MSB MSB MSB MSB
DP X X dp dp dp dp dp dp dp
UX X X X Hz X X X X MHz
X = Doesn't matter
DP = Decimal Point follows digit when dp = 1. Only one dp = 1 per reading. All others = 0.
UX = Measurement unit occurs as indicated when bit = 1. Only one UX bit = 1 per reading. All others = 0 or are ignored.

Figure 521-4. 7220A Data Transfer Format and Timing

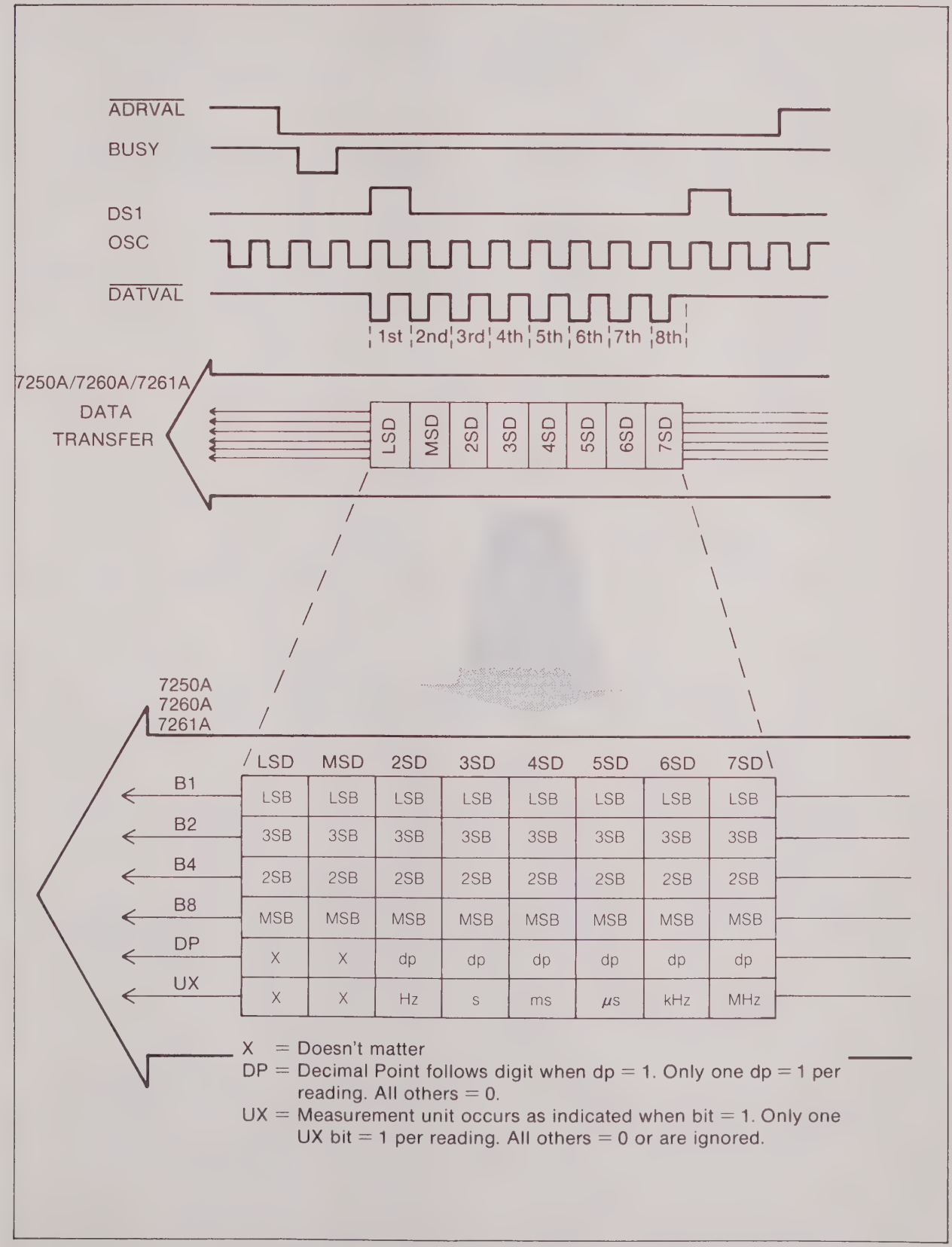

ADRVAL
BUSY
DS1
OSC
DATVAL
1st 2nd 3rd 4th 5th 6th 7th 8th
7250A/7260A/7261A
DATA
TRANSFER
LSD MSD 2SD 3SD 4SD 5SD 6SD 7SD
7250A
7260A
7261A
LSD MSD 2SD 3SD 4SD 5SD 6SD 7SD
B1 LSB LSB LSB LSB LSB LSB LSB LSB
B2 3SB 3SB 3SB 3SB 3SB 3SB 3SB 3SB
B4 2SB 2SB 2SB 2SB 2SB 2SB 2SB 2SB
B8 MSB MSB MSB MSB MSB MSB MSB MSB
DP X X dp dp dp dp dp dp
UX X X Hz s ms μs kHz MHz
X = Doesn't matter
DP = Decimal Point follows digit when dp = 1. Only one dp = 1 per reading. All others = 0.
UX = Measurement unit occurs as indicated when bit = 1. Only one UX bit = 1 per reading. All others = 0 or are ignored.

Figure 521-5. 7260A, 7261A, 7250A Data Transfer Format and Timing

Table 521-1. Data Format Example

7250A frequency measurement of 537.387 kHz made in the FREQ A mode with 1 Hz resolution.

	LSD	MSD	2SD	3SD	4SD	5SD	6SD	7SD
B1	1	0	0	1	1	1	1	0
B2	1	0	0	0	1	1	1	0
B4	1	0	0	1	0	1	0	0
B8	0	0	0	0	0	0	0	1
DP	x	x	0	0	0	1	0	0
UX	x	x	0	0	0	0	1	0

x=Doesn't matter

The printer output looks like this:

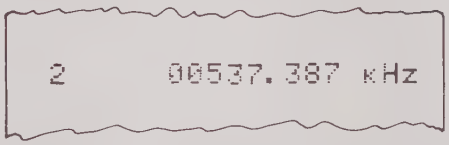


Table 521-2. Troubleshooting Guide-Printer Interface

CHECK:		YOU SHOULD SEE:
Connector J4	Pin 2	+5V (supplied by counter)
Address Decode	U2-5	Positive pulse (CMOS) each time the printer addresses the counter.
U1 Buffer Enable	U3-4	Negative pulse, inverse of pulse on U2-5.
BUSY (BY)	U2-3	Pulses from counter indicating measurement is complete.
	U2-1	Positive pulse, one per print command. Occurs at completion of measurement.
	U2-11	Positive pulses, DSI from display.
	U2-13	Positive pulse, one per print command. Goes high at beginning of DSI, falls at beginning of next DSI.
$\overline{\text{DATVAL}}$	U4-11	Burst of 8 negative pulses (9 for the 7220A), one burst per print command.

521-36. Pin Assignment Table

521-37. Table 521-3 provides a list of the pin assignments for P5, which is the connection at the rear panel of the counter between the Digital Interface PCB and the cable to the printer. For pin assignments for J4, the connection between the Digital Interface PCB and the Main PCB of the counter, see the schematic in Section 8 of the Counter Instruction Manual.

521-38. REPLACEABLE PARTS

521-39. A detailed list of replaceable parts is presented in Table 521-4. Figure 521-6 can be used as an aid in locating components. Refer to Section 5 of the counter instruction manual for parts ordering information.

Table 521-3. P5 Pin Assignments.

P5 PIN NO.	MNEMONIC	SOURCE		DESCRIPTION
		COUNTER	PRINTER	
1	$\overline{\text{ADRVAL}}$	X		Address Valid
2	$\overline{\text{DATVAL}}$	X		Data Valid
3	A0		X	LSB (Counter Address)
4	A1		X	3SB (Counter Address)
5	A2		X	2SB (Counter Address)
6	A3		X	MSB (Counter Address)
7	not used			
8	not used			
9	D0	X		BCD Bit 1
10	D1	X		BCD Bit 2
11	D2	X		BCD Bit 4
12	D3	X		BCD Bit 8
13	D4	X		Decimal Point (DP)
14	D5	X		Measurement Unit (UX)
15	not used			
16	not used			
17	GND			
18	+5V Supplied by printer			
19-36	not used			

Note: $\overline{\text{BUSEN}}$ (pin no. 22) is always held high when the Printer Interface is used with a printer.

Table 521-4. Digital Interface (Option -521)

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	NOTE
	⊘ DIGITAL INTERFACE, OPTION-521 FIGURE 6521-6 (7220A-4007T)	ORDER	BY	OPTION -521	1		
J4	CONNECTOR, 36-PIN	484733	00779	87406-1	1		
P5	CONNECTOR, 36-PIN	479493	00779	552817-1	1		
RN1	RESISTOR NETWORK, 100K	461038	89536	461038	1	1	
U1⊘	IC, C-MOS, HEX NON INVET BUFFERS	407759	04713	MC14503CP	3	1	
U2⊘	IC, C-MOS, DUAL TYPE "D" FLIP-FLOP	340117	04713	MC14013CP	1	1	
U3⊘	IC, C-MOS, QUAD, 2-INPUT NAND GATES	355198	04713	MC14011CP	1	1	
U4	IC, TRI-STATE HEX BUFFER	483800	01295	SN74LS367N	1	1	
U5⊘	IC, C-MOS, BCD TO DECIMAL DECODER	380741	01295	TP4028AN	1	1	
U6	IC, LO-PWR, SCHOTTKY TRI-ST OCTAL, BFR.	429902	12040	DM81LS95N	1	1	
U7⊘	IC, C-MOS, HEX NON INVET BUFFERS	407759	04713	MC14503CP	REF		
U8⊘	IC, C-MOS, HEX NON INVET BUFFERS	407759	04713	MC14503CP	REF		
W1	PLUG, JUMPER	416842	91506	8136-651P2	1		
W1.	SOCKETS	376418	89536	376418	13		

NOTE: ⊘ Indicates the item can be damaged by static discharge.

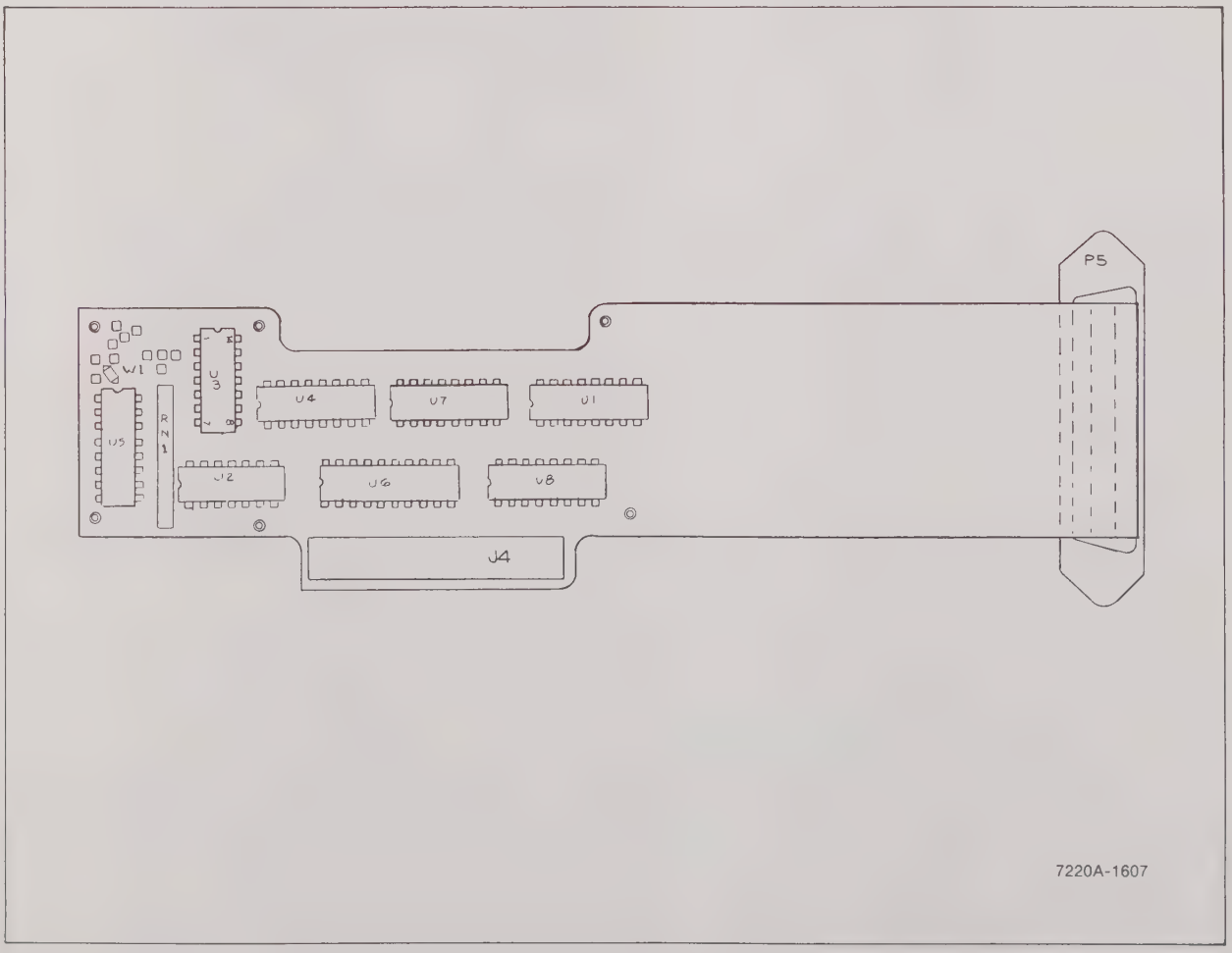


Figure 521-6. Digital Interface (Option -521)

Section 7
General Information

7-1. This section of the manual contains generalized user information as well as supplemental information to the List of Replaceable Parts contained in Section 5.

List of Abbreviations and Symbols

A or amp	ampere
ac	alternating current
af	audio frequency
a/d	analog-to-digital
assy	assembly
AWG	american wire gauge
B	bel
bcd	binary coded decimal
°C	Celsius
cap	capacitor
ccw	counterclockwise
cer	ceramic
cermet	ceramic to metal(seal)
ckt	circuit
cm	centimeter
cmrr	common mode rejection ratio
comp	composition
cont	continue
crt	cathode-ray tube
cw	clockwise
d/a	digital-to-analog
dac	digital-to-analog converter
dB	decibel
dc	direct current
dmm	digital multimeter
dvm	digital voltmeter
elect	electrolytic
ext	external
F	farad
°F	Fahrenheit
FET	Field-effect transistor
ff	flip-flop
freq	frequency
FSN	federal stock number
g	gram
G	giga (10^9)
gd	guard
Ge	germanium
GHz	gigahertz
gmv	guaranteed minimum value
gnd	ground
H	henry
hd	heavy duty
hf	high frequency
Hz	hertz
IC	integrated circuit
if	intermediate frequency
in	inch(es)
intl	internal
I/O	input/output
k	kilo (10^3)
kHz	kilohertz
kΩ	kilohm(s)
kV	kilovolt(s)
lf	low frequency
LED	light-emitting diode
LSB	least significant bit
LSD	least significant digit
M	mega (10^6)
m	milli (10^{-3})
mA	milliampere(s)
max	maximum
mf	metal film
MHz	megahertz
min	minimum
mm	millimeter
ms	millisecond
MSB	most significant bit
MSD	most significant digit
MTBF	mean time between failures
MTTR	mean time to repair
mV	millivolt(s)
mv	multivibrator
MΩ	megohm(s)
n	nano (10^{-9})
na	not applicable
NC	normally closed
(–) or neg	negative
NO	normally open
ns	nanosecond
opnl ampl	operational amplifier
p	pico (10^{-12})
para	paragraph
pcb	printed circuit board
pF	picofarad
pn	part number
(+) or pos	positive
pot	potentiometer
p-p	peak-to-peak
ppm	parts per million
PROM	programmablle read-only memory
psi	pound-force per square inch
RAM	random-access memory
rf	radio frequency
rms	root mean square
ROM	read-only memory
s or sec	second (time)
scope	oscilloscope
SH	shield
Si	silicon
serno	serial number
sr	shift register
Ta	tantalum
tb	terminal board
tc	temperature coefficient or temperature compensating
tcxo	temperature compensated crystal oscillator
tp	test point
u or μ	micro (10^{-6})
uhf	ultra high frequency
us or μs	microsecond(s) (10^{-6})
uut	unit under test
V	volt
v	voltage
var	variable
vco	voltage controlled oscillator
vhf	very high frequency
vlf	very low frequency
W	watt(s)
ww	wire wound
xfmr	transformer
xstr	transistor
xtal	crystal
xtlo	crystal oscillator
Ω	ohm(s)
μ	micro (10^{-6})

Federal Supply Codes for Manufacturers

D9816
Westermann Wilhelm Augusta-Anlage
Mannheim-Nackarau Germany

00199
Marcon Electronics Corp
Kearny, New Jersey

00213
Nytronics Comp. Group Inc.
Darrlington, South Carolina

00327
Welwyn International Inc.
Westlake, Ohio

00656
Aerovox Corp.
New Bedford, Massachusetts

00686
Film Capacitors Inc.
Passaic, New Jersey

00779
AMP, Inc.
Harrisburg, Pennsylvania

01121
Allen Bradley Co.
Milwaukee, Wisconsin

01281
TRW Electronics & Defense Sector
Lawndale, California

01295
Texas Instruments Inc.
Semiconductor Group
Dallas,Texas

01537
Motorola Communications &
Electronics Inc.
Franklin Park, Illinois

01686
RCL Electronics/Shallcross Inc.
Electro Components Div.
Manchester, New Hampshire

01884
Sprague Electric Co.
(Now 56289)

01961
Varian Associates Inc.
Pulse Engineering Div.
Convoy, Connecticut

02111
Spectrol Electronics Corp.
City of Industry, California

02114
Amperex Electronic Corp.
Ferrox Cube Div.
Saugerties, New York

02131
General Instrument Corp.Government
Systems Div.
Westwood, Massachusetts

02395
Sonar Radio Corp.
Hollywood, Florida

02533
Leigh Instruments Ltd.
Frequency Control Div.
Don Mills, Ontario, Canada

02606
Fenwal Labs
Division of Travenal Labs
Morton Grove, Illinois

0266
Bunker Ramo-Eltra Corp.
Amphenol NA Div.
Broadview, Illinois

02735
RCA-Solid State Div.
Somerville, New Jersey

02799
Arco Electronics Inc.
Chatsworth, California

03508
General Electric Co.
Semiconductor Products& Batteries
Aubum, New York

03797
Genisco Technology Corp.
Eltronics Div.
Rancho Dominquez, Calif.

03877
Gilbert Engineering Co.Inc
Incon Sub of Transitron
Electronic Corp.
Glendale, Arizona

03888
KDI Electronics Inc.
Pyrofilm Div.
Whippany, New Jersey

03911
Clairex Corp.
Clairex Electronics Div.
Mount Vernon, New York

03980
Muirhead Inc.
Mountainside, New Jersey

04009
Cooper Industries, Inc.
Arrow Hart Div.
Hartford, Connecticut

04217
Essex International Inc.
Wire & Cable Div.
Anaheim, California

04221
Midland-Ross Corp.
Midtex Div.
N. Mankato, Minnesota

04222
AVX Corp.
AVX Ceramics Div.
Myrtle Beach, S. Carolina

04423
Telonic Berkley Inc.
Laguna Beach, California

04713
Motorola Inc.
Semiconductor Group
Phoenix, Arizona

05236
Jonathan Mfg. Co.
Fullerton, California

05245
Corcom Inc.
Libertyville, Illinois

05276
ITT Pomona
Electronics Div.
Pomona, California

05277
Westinghouse Elec. Corp.
Semiconductor Div.
Youngwood, Pennsylvania

05397
Union Carbide Corp.
Materials Systems Div.
Cleveland. Ohio

05571
Sprague Electric Co.
(Now 56289)

05574
Viking Connectors Inc
Sub of Criton Corp.
Chatsworth, Calif.

05820
EG & G Wakefield Engineering
Wakefield, Massachusetts

05972
Loctite Corp.
Newington, Connecticut

06001
General Electric Co.
Electric Capacitor Product Section
Columbia, S. Carolina

06141
Fairchild Weston Systems Inc.
Data Systems Div.
Sarasota, Florida

06192
La Deau Mfg. Co.
Glendale, California

06229
Electrovert Inc.
Elmsford, New York

06383
Panduit Corp.
Tinley Park, Illinois

06473
Bunker Ramo Corp.
Amphenol NA Div.
SAMS Operation
Chatsworth, California

06555
Beede Electrical Instrument
Penacook, New Hampshire

06665
Precision Monolithics
Sub of Bourns Inc.
Santa Clara, California

06666
General Devices Co. Inc.
Indianapolis, Indiana

06739
Electron Corp.
Littleton, Colorado

06743
Gould Inc.
Foil Div.
Eastlake, Ohio

06751
Components Inc.
Semcor Div.
Phoenix, Arizona

06776
Robinson Nugent Inc.
New Albany, Indiana

06915
Richco Plastic Co.
Chicago, Illinois

06961
Vemitron Corp.
Piezo Electric Div.
Bedford, Ohio

06980
Varian Associates Inc.
Eimac Div.
San Carlos, California

07047
Ross Milton Co., The
Southampton, Penna.

07138
Westinghouse Electric Corp.
Industrial & Government
Tube Div.
Horseheads, New York

07233
Benchmark Technology Inc.
City of Industry, Calif.

07239
Biddle Instruments
Blue Bell, Penna.

07256
Silicon Transistor Corp.
Sub of BBF Inc.
Chelmsford, Massachusetts

07261
Avnet Corp.
Culver City, California

07263
Fairchild Camera & Instrument
Semiconductor Div.
Mountain View, California

07344
Bircher Co. Inc., The
Rochester, New York

Federal Supply Codes for Manufacturers (cont)

07557
Campion Co. Inc.
Philadelphia, Penna.

07597
Burndy Corp.
Tape/Cable Div.
Rochester, New York

07716
TRW Inc. (Can use 11502)
IRC Fixed Resistors/
Burlington
Burlington, Iowa

07792
Lemna Engineering Corp.
Northampton, Massachusetts

07810
Bock Corp.
Madison, Wisconsin

07933
Raytheon Co.
Semiconductor Div.
Mountain View, Calif.

08235
Industro Transistor Corp.
Long Island City, New York

08261
Spectra-Strip
An Eltra Co.
Garden Grove, Calif.

08530
Reliance Mica Corp.
Brooklyn, New York

08718
ITT Cannon Electric
Phoenix Div.
Phoenix, Arizona

08806
General Electric Co.
Minature Lamp Products
Cleveland, Ohio

08863
Nylomatic
Fallsington, Penna.

08988
Skottie Electronics Inc.
Archbald, Pennsylvania

09021
Airco Inc.
Airco Electronics
Bradford, Penna.

09023
Cornell-Dublier Electronics
Fuquay-Varina, N. Carolina

09214
General Electric Co.
Semiconductor Products Dept.
Auburn, New York

09353
C and K Components Inc.
Newton, Massachusetts

09423
Scientific Components Inc.
Santa Barbara, California

09579
CTS of Canada, Ltd
Streetsville, Ontario

09922
Burndy Corp.
Norwalk, Connecticut

09969
Dale Electronics Inc.
Yankton, South Dakota

09975
Burroughs Corp.
Electronics Components
Detroit, Michigan

10059
Barker Engineering Corp.
Kenilworth, New Jersey

10389
Illinois Tool Works Inc.
Licon Div.
Chicago, Illinois

10582
CTS of Asheville
Skyland, N. Carolina

11236
CTS Corp.
Berne Div.
Berne, Indiana

11237
CTS Corp of California
Paso Robles Div.
Paso Robles, California

11295
ECM Motor Co.
Schaumburg, Illinois

11358
Columbia Broadcasting System
CBS Electronic Div.
Newburyport, Massachusetts

11403
Vacuum Can Co.Best Coffee Maker Div.
Chicago, Illinois

11502
TRW Inc.
TRW Resistive Products Div.
Boone, North Carolina

11503
Keystone Columbia Inc.
Freemont, Indiana

11532
Teledyne Relays Teledyne
Industries Inc.
Hawthorne, California

11711
General Instrument Corp.
Rectifier Div.
Hicksville, New York

11726
Qualidyne Corp.
Santa Clara, California

12014
Chicago Rivet & Machine Co.
Naperville, Illinois

12040
National Semiconductor Corp.
Danbury, Connecticut

12060
Diodes Inc.
Northridge, California

12136
PHC Industries Inc.
Formerly Philadelphia Handle Co.
Camden, New Jersey

12300
AMF Canada Ltd.
Potter-Brumfield
Guelph, Ontario, Canada

12323
Practical Automation Inc.
Shelton, Connecticut

12327
Freeway Corp.
Cleveland, Ohio

12443
Budd Co.,The
Plastics Products Div.
Phoenixville, Pennsylvania

12581
Hitachi Metals International Ltd.
Hitachi Magna-Lock Div.
Big Rapids, Missouri

12615
US Terminals Inc.
Cincinnati, Ohio

12617
Hamlin Inc.
Lake Mills, Wisconsin

12697
Clarostat Mfg. Co. Inc.
Dover, New Hampshire

12749
James Electronic Inc.
Chicago, Illinois

12856
MicroMetals Inc.
Anaheim, California

12881
Metex Corp.
Edison, New Jersey

12895
Cleveland Electric Motor Co.
Cleveland, Ohio

12954
Microsemi Corp.
Components Group
Scottsdale, Arizona

12969
Unitrode Corp.
Lexington, Massachusetts

13050
Potter Co.
Wesson, Mississippi

13103
Thermalloy Co., Inc.
Dallas, Texas

13327
Solitron Devices Inc.
Tappan, New York

13511
Bunker-Ramo Corp.
Amphenol Cadre Div.
Los Gatos, California

13606
Sprague Electric Co.
(Use 56289)

13689
SPS Technologies Inc.
Hatfield, Pennsylvania

13919
Burr-Brown Research Corp.
Tucson, Arizona

14099
Semtech Corp.
Newbury Park, California

14140
McGray-Edison Co.
Commercial Development Div.
Manchester, New Hampshire

14193
Cal-R-Inc.
Santa Monica, California

14298
American Components Inc.
an Insilco Co. RPC Div.
Conshohocken, Pennsylvania

14298
ACIC Inc.
Sub of Insilco Corp.
Research Triangle Park, NC

14329
Wells Electronics Inc.
South Bend, Indiana

14482
Watkins-Johnson Co.
Palo Alto, California

14552
Microsemi Corp.
Santa Ana, California

14655
Cornell-Dublier Electronics
Div. of Federal Pacific
Electric Co. Govt Cont Dept.
Newark, New Jersey

Federal Supply Codes for Manufacturers (cont)

14704
Crydom Controls
(Division of Int Rectifier)
El Segundo, California

14752
Electro Cube Inc.
San Gabriel, California

14936
General Instrument Corp.
Discrete Semi Conductor Div.
Hicksville, New York

14949
Trompeter Electronics
Chatsworth, California

15412
Amtron
Midlothian, Illinois

15542
Scientific Components Corp.
Mini-Circuits Laboratory Div.
Brooklyn, New York

15636
Elec-Trol Inc.
Saugus, California

15782
Bausch & Lomb Inc.
Graphics & Control Div.
Austin, Texas

15801
Fenwal Eletronics Inc.
Div. of Kidde Inc.
Framingham, Massachusetts

15818
Teledyne Inc. Co.
Teledyne Semiconductor Div.
Mountain View, California

15849
Useco Inc.
(Now 88245)

15898
International Business
Machines Corp.
Essex Junction, Vermont

16245
Conap Inc.
Olean, New York

16258
Space-Lok Inc.
Burbank, California

16352
Codi Corp.
Linden, New Jersey

16469
MCL Inc.
LaGrange, Illinois

16473
Cambridge Scientific Industries
Div. of Chemed Corp.
Cambridge, Maryland

16733
Cablewave Systems Inc.
North Haven, Connecticut

16742
Paramount Plastics
Fabricators Inc.
Downey, California

16758
General Motors Corp.
Delco Electronics Div.
Kokomo, Indiana

17069
Circuit Structures Lab
Burbank, California

17117
Electronic Molding Corp.
Woonsocket, Rhode Island

17338
High Pressure Eng. Co. Inc.
Oklahoma City, Oklahoma

17545
Atlantic Semiconductors Inc.
Asbury Park, New Jersey

17745
Angstrohm Precision, Inc.
Hagerstown, Maryland

17856
Siliconix Inc.
Santa Clara, California

18178
E G & Gvactee Inc.
St. Louis, Missouri

18324
Signetics Corp.
Sacramento, California

18520
Sharp Electronics Corp.
Paramus, New Jersey

18542
Wabash Inc.
Wabash Relay & Electronics Div.
Wabash, Indiana

18565
Chomerics Inc.
Woburn, Massachusetts

18612
Vishay Intertechnology Inc.
Vishay Resistor Products Group
Malvern, Pennsylvania

18632
Norton-Chemplast
Santa Monica, California

18677
Scanbe Mfg. Co.
Div. of Zero Corp.
El Monte, California

18736
Voltronics Corp.
East Hanover, New Jersey

18927
GTE Products Corp.
Precision Material Products
Business Parts Div.
Titusville, Pennsylvania

19315
Bendix Corp., The
Navigation & Control Group
Terboro, New Jersey

19451
Perine Machinery & Supply Co..
Kent, Washington

19613
Minnesota Mining & Mfg. Co.
Textool Products Dept.
Electronic Product Div.
Irving, Texas

19647
Caddock Electronics Inc.
Riverside, California

19701
Mepco/Centralab Inc.
A N. American Philips Co.
Mineral Wells, Texas

20584
Enochs Mfg. Inc.
Indianapolis, Indiana

20891
Cosar Corp.
Dallas, Texas

21317
Electronics Applications Co.
El Monte, California

21604
Buckeye Stamping Co.
Columbus, Ohio

21845
Solitron Devices Inc.
Semiconductor Group
Rivera Beach, Florida

22526
DuPont, EI DeNemours & Co. Inc.
DuPont Connector Systems
Advanced Products Div.
New Cumberland, Pennsylvania

22767
ITT Semiconductors
Palo Alto, California

22784
Palmer Inc.
Cleveland, Ohio

23050
Product Comp. Corp.
Mount Vernon, New York

23732
Tracor Applied Sciences Inc.
Rockville, Maryland

23880
Stanford Applied Engineering
Santa Clara, California

23936
William J. Purdy Co.
Pamotor Div.
Burlingame, California

24347
Penn Engineering Co.
S. El Monte, California

24355
Analog Devices Inc.
Norwood, Massachusetts

24444
General Semiconductor
Industries, Inc.
Tempe, Arizona

24655
Genrad Inc.
Concord, Massachusetts

24759Lenox-Fugle Electronics Inc.
South Plainfield, New Jersey

24796
AMF Inc.
Potter & Brumfield Div.
San Juan Capistrano, Calif.

24931
Specialty Connector Co.
Greenwood, Indiana

25088
Siemen Corp.
Isilen, New Jersey

25099
Cascade Gasket
Kent, Washington

25403
Amperex Electronic Corp.
Semiconductor & Micro-Circuit Div.
Slatersville, Rhode Island

25706
Daburn Electronic & Cable Corp.
Norwood, New Jersey

26629
Frequency Sources Inc.
Sources Div.
Chelmsford, Massachusetts

26806
American Zettler Inc.
Irvine, California

27014
National Semiconductor Corp.
Santa Clara, California

27167
Corning Glass Works Corning
Electronics
Wilmington, North Carolina

27264
Molex Inc.
Lisle, Illinois

27440
Industrial Screw Products
Los Angeles, California

Federal Supply Codes for Manufacturers (cont)

27745
Associated Spring Barnes Group Inc.
Syracuse, New York

27956
Relcom (Now 14482)

28198
Positronic Industries
Springfield, Missouri

28213
Minnesota Mining & Mfg. Co.
Consumer Products Div.
3M Center
Saint Paul, Minnesota

28425
Serv-O-Link
Euless, Texas

28478
Deltrol Corporation
Deltrol Controls Div.
Milwaukee, Wisconsin

28480
Hewlett Packard Co.
Corporate HQ
Palo Alto, California

28484
Emerson Electric Co.
Gearmaster Div.
McHenry, Illinois

28520
Heyco Molded Products
Kenilworth, New Jersey

29083
Monsanto Co.
Santa Clara, California

29604
Stackpole Components Co.
Raleigh, North Carolina

29907
Omega Engineering Inc.
Stamford, Connnecticut

30035
Jolo Industries Inc.
Garden Grove, California

30146
Symbex Corp.
Painesville, Ohio

30148
AB Enterprise Inc.
Ahoskie, North Carolina

30161
Aavid Engineering Inc.
Laconia, New Hampshire

30315
Itron Corp.
San Diego, California

30323
Illinois Tool Works Inc.
Chicago, Illinois

30800
General Instrument Corp.
Capacitor Div.
Hicksville, New York

31019
Solid State Scientific Inc.
Willow Grove, Pennsylvania

31091
Alpha Industries Inc.
Microelectronics Div.
Hatfield, Pennsylvania

31323
Metro Supply Company
Sacramento, California

31448
Army Safeguard Logistics Command
Huntsville, Alabama

31746
Cannon Electric
Woodbury, Tennessee

31827
Budwig
Ramona, California

31918
ITT-Schadow
Eden Prairie, Minnesota

32293
Intersil
Cupertino, California

32539
Mura Corp.
Westbury, Long Island, N.Y.

32559
Bivar
Santa Ana, California

32767
Griffith Plastics Corp.
Burlingame, California

32879
Advanced Mechanical Components
Northridge, California

32897
Murata Erie North America Inc.
Carlisle Operations
Carlisle, Pennsylvania

32997
Bourns Inc.
Trimpot Div.
Riverside, California

33096
Colorado Crystal Corp.
Loveland, Colorado

33173
General Electric Co.
Owensboro, Kentucky

33246
Epoxy Technology Inc.
Billerica, Massachusetts

33297
NEC Electronics USA Inc.
Electronic Arrays Inc. Div.
Mountain View, California

33919
Nortek Inc.
Cranston, Rhode Island

34333
Silicon General Inc.
Garden Grove, California

34225
Advanced Micro Devices
Sunnyvale, California

34359
Minnesota Mining & Mfg. Co.
Commercial Office Supply Div.
Saint Paul, Minnesota

34371
Harris Corp.
Harris Semiconductor
Products Group
Melbourne, Florida

34649
Intel Corp.
Santa Clara, California

34802
Electromotive Inc.
Kenilworth, New Jersey

34848
Hartwell Special Products
Placentia, California

35009
Renfrew Electric Co. Ltd.
IRC Div.
Toronto, Ontario, Canada

36665
Mitel Corp.
Kanata, Ontario, Canada

37942
Mallory Capacitor Corp.
Sub of Emhart Industries
Indianapolis, Indiana

39003
Maxim Industries
Middleboro, Massachusetts

40402
Roderstein Electronics Inc.
Statesville, North Carolina

42498
National Radio
Melrose, Massachusetts

43543
Nytronics Inc.(Now 53342)

44655
Ohmite Mfg. Co.
Skokie, Illinois

49671
RCA Corp.
New York, New York

49956
Raytheon Company
Executive Offices
Lexington, Massachusetts

50088
Thomson Components-Mostek Corp.
Carrollton, Texas

50120
Eagle-Picher Industries Inc.
Electronics Div.
Colorado Springs, Colorado

50157
Midwest Components Inc.
Muskegon, Mississippi

50541
Hypertronics Corp.
Hudson, Massachusetts

50579
Litronix Inc.
Cupertino, California

51167
Aries Electronics Inc.
Frenchtown, New Jersey

51372
Verbatim Corp.
Sunnyvale, California

51406
Murata Erie, No. America Inc.
(Also see 72982)
Marietta, Georgia

51499
Amtron Corp.
Boston, Massachusetts

51605
CODI Semiconductor Inc.
Kenilworth, New Jersey

51642
Centre Engineering Inc.
State College, Pennsylvania

51791
Statek Corp.
Orange, California

51984
NEC America Inc.
Falls Church, Virginia

52063
Exar Integrated Systems
Sunnyvale, California

52072
Circuit Assembly Corp.
Irvine, California

52152
Minnesota Mining & Mfg.
Saint Paul, Minnesota

52333
API Electronics
Haugpauge,Long Island,New York

Federal Supply Codes for Manufacturers (cont)

52361
Communication Systems
Piscataway, New Jersey

52525
Space-Lok Inc.
Lerco Div.
Burbank, California

52531
Hitachi Magnetics
Edmore, Missouri

52745
Timco
Los Angeles, California

52763
Stettner-Electronics Inc.
Chattanooga, Tennessee

52769
Sprague-Goodman Electronics Inc.
Garden City Park, New York

52771
Moniterm Corp.
Amatrom Div.
Santa Clara, California

52840
Western Digital Corp.
Costa Mesa, California

53021
Sangamo Weston Inc.
(See 06141)

53217
Technical Wire Products Inc.
Santa Barbara, California

53342
Opt Industries Inc.
Phillipsburg, New Jersey

53944
Glow-Lite
Pauls Valley, Oklahoma

54294
Shallcross Inc.
Smithfield, North Carolina

54453
Sullins Electronic Corp.
San Marcos, California

54473
Matsushita Electric Corp.
(Panasonic)
Secaucus, New Jersey

54583
TDK
Garden City, New York

54869
Piher International Corp.
Arlington Heights, Illinois

54937
DeYoung Mfg.
Bellevue, Washington

54590
RCA Corp.
Electronic Components Div.
Cherry Hill, New Jersey

55026
American Gage & Machine Co.
Simpson Electric Co. Div.
Elgin, Illinois

55112
Plessey Capacitors Inc.
(Now 60935)

55261
LSI Computer Systems Inc.
Melville, New York

55285
Bercquist Co.
Minneapolis, Minnesota

55576
Synertek
Santa Clara, California

55680
Michicon/America/Corp.
Schaumburg, Illinois

56282
Utek Systems Inc.
Olathe, Kansas

56289
Sprague Electric Co.
North Adams, Massachusetts

56365
Square D Co.
Corporate Offices
Palatine, Illinois

56375
DAL Industries Inc.
Wescorp Div.
Mountain View, California

56481
Shugart Associates
Sub of Xerox Corp.
Sunnyvale, California

56708
Zilog Inc.
Campbell, California

56856
Varistor Corp. of Tennessee
Sevierville, Tennessee

56880
Magnetics Inc.
Baltimore, Maryland

57026
Endicott Coil Co. Inc.
Binghamton, New York

57053
Gates Energy Products
Denver, Ohio

58014
Hitachi Magnalock Corp.
(Now 12581)

58104
Simco
Atlanta, Georgia

58474
Superior Electric Co.
Bristol, Connecticut

59124
KOA-Speer Electronics Inc.
Bradford, Pennsylvania

59640
Supertex Inc.
Sunnyvale, California

59660
Tusonix Inc.
Tucson, Arizona

59730
Thomas and Betts Corp.
Iowa City, Iowa

59831
Semtronics Corp.
Watchung, New Jersey

60395
Xicor Inc.
Milpitas, California

60399
Torin Engineered Blowers
Div. of Clevepak Corp.
Torrington, Connecticut

60705
Cera-Mite Corp.
(formerly Sprague)
Grafton, Wisconsin

60935
Westlake Capacitor Inc.
Tantalum Div.
Greencastle, Indiana

61804
M/A Com Inc.
Burlington, Massachusetts

61857
SAN-O Industrial Corp.
Bohemia, Long Island, NY

61935
Schurter Inc.
Petaluma, California

62351
Apple Rubber
Lancaster, New York

62793
Lear Siegler Inc.
Energy Products Div.
Santa Ana, California

63743
Ward Leonard Electric Co.Inc.
Mount Vernon, New York

64154
Lamb Industries
Portland, Oregon

64155
Linear Technology
Milpitas, California

64834
West M G Co.
San Francisco, Calif.

65092
Sangamo Weston Inc.
Weston Instruments Div.
Newark, New Jersey

65940
Rohm Corp & Whatney
Irvine, California

65964
Evox Inc.
Bannockburn, Illinois

66150
Entron Inc.
Winslow Teltronics Div.
Glendale, New York

66608
Bering Industries
Fremont, California

70290
Almetal Universal Joint Co.
Cleveland, Ohio

70485
Atlantic India Rubber Works Inc.
Chicago, Illinois

70563
Amperite Company
Union City, New Jersey

70903
Belden Corp.
Geneva, Illinois

71002
Birnbach Co. Inc.
Farmingdale, New York

71034
Bliley Electric Co.
Erie, Pennsylvania

71183
Westinghouse Electric Corp.
Bryant Div.
Bridgeport, Connecticut

71400
Bussman Manufacturing
Div. McGraw-Edison Co.
St. Louis, Missouri

71450
CTS Corp.
Elkhart, Indiana

71468
ITT Cannon Div. of ITT
Fountain Valley, California

71482
General Instrument Corp.
Clare Div.
Chicago, Illinois

Federal Supply Codes for Manufacturers (cont)

71590
Mepco/Centralab
A North American Philips Co.
Fort Dodge, Iowa

71707
Coto Corp.
Providence, Rhode Island

71744
General Instrument Corp.
Lamp Div/Worldwide
Chicago, Illinois

71785
TRW Inc.
Cinch Connector Div.
Elk Grove Village, Illinois

71984
Dow Corning Corp.
Midland, Michigan

72005
AMAX Specialty Metals Corp.
Newark, New Jersey

72136
Electro Motive Mfg. Corp.
Florence, South Carolina

72228
AMCA International Corp.
Continental Screw Div.
New Bedford, Massachusetts

72259
Nytronics Inc.
New York, New York

72619
Amperex Electronic Corp.
Dialight Div.
Brooklyn, New York

72653
G C Electronics Co.
Div. of Hydrometals Inc.
Rockford, Illinois

72794
Dzus Fastner Co. Inc.
West Islip, New York

72928
Gulton Industries Inc.
Gudeman Div.
Chicago, Illinois

72982
Murata Erie N. America Inc.
Erie, Pennsylvania

73138
Beckman Industrial corp.
Helipot Div.
Fullerton, California

73168
Fenwal Inc.
Ashland, Massachusetts

73293
Hughes Aircraft Co.
Electron Dynamics Div.
Torrance, California

73445
Amperex Electronic Corp.
Hicksville, New York

73559
Carlingswitch Inc.
Hartford, Connecticut

73586
Circle F Industries
Trenton, New Jersey

73734
Federal Screw Products Inc.
Chicago, Illinois

73743
Fischer Special Mfg. Co.
Cold Spring, Kentucky

73893
Microdot
Mt. Clemens, Mississippi

73899
JFD Electronic Components
Div. of Murata Erie
Oceanside, New York

73905
FL Industries Inc.
San Jose, California

73949
Guardian Electric Mfg. Co.
Chicago, Illinois

74199
Quam Nichols Co.
Chicago, Illinois

74217
Radio Switch Co.
Marlboro, New Jersey

74306
Piezo Crystal Co.
Div. of PPA Industries Inc.
Carlisle, Pennsylvania

74542
Hoyt Elect.Instr. Works Inc.
Penacook, New Hampshire

74840
Illinois Capacitor Inc.
Lincolnwood, Illinois

74970
Johnson EF Co.
Waseca, Minnesota

75042
TRW Inc.
IRC Fixed Resistors
Philadelphia, Pennsylvania

75297
Litton Systems
Kester Solder Div.
Chicago, Illinois

75376
Kurz-Kasch Inc.
Dayton, Ohio

75378
CTS Knights Inc.
Sandwich, Illinois

75382
Kulka Electric Corp.
(Now 83330)
Mount Vernon, New York

75915
Tracor Littlefuse
Des Plaines, Illinois

76854
Oak Switch Systems Inc.
Crystal Lake, Illinois

77122
TRW Assemblies & Fasteners Group
Fastener Div.
Moutainside, New Jersey

77342
AMF Inc.
Potter & Brumfield Div.
Princeton, Indiana

77542
Ray-O-Vac Corp
Madison, Wisconsin

77638
General Instrument Corp.
Rectifier Div.
Brooklyn, New York

77900
Shakeproof Lock Washer Co.
(Now 78189)

77969
Rubbercraft Corp. of CA Ltd.
Torrance, California

78189
Illinois Tool Works Inc.
Shakeproof Div.
Elgin, Illinois

78277
Sigma Instruments Inc.
South Braintree, Mass.

78290
Struthers Dunn Inc.
Pitman, New Jersey

78553
Eaton Corp.
Engineered Fastener Div.
Cleveland, Ohio

78592
Stoeger Industries
South Hackensack, New Jersey

79136
Waldes Kohinoor Inc.
Long Island City, New York

79497
Western Rubber Co.
Goshen, Indiana

79727
C - W Industries
Southampton, Pennsylvania

79963
Zierick Mfg. Corp.
Mount Kisco, New York

80009
Tektronix
Beaverton, Oregon

80031
Mepco/Electra Inc.
Morristown, New Jersey

80032
Ford Aerospace & Communications Corp.
Western Development
Laboratories Div.
Palo Alto, California

80145
LFE Corp.
Process Control Div.
Clinton, Ohio

80183
Sprague Products
(Now 56289)

80294
Bourns Instruments Inc.
Riverside, California

80583
Hammerlund Mfg. Co. Inc.
Paramus, New Jersey

80640
Computer Products Inc.
Stevens-Arnold Div.
South Boston, Mass.

81073
Grayhill Inc.
La Grange, Illinois

81312
Litton Systems Inc.
Winchester Electronics Div.
Watertown, Connecticut

81439
Therm-O-Disc Inc.
Mansfield, Ohio

81483
International Rectifier Corp.
Los Angeles, California

81590
Korry Electronics Inc.
Seattle, Washington

81741
Chicago Lock Co.
Chicago, Illinois

82227
Airpax Corp.
Cheshire Div.
Cheshire, Connecticut

82240
Simmons Fastner Corp.
Albany, New York

Federal Supply Codes for Manufacturers (cont)

82305
Palmer Electronics Corp.
South Gate, California

82389
Switchcraft Inc.
Sub of Raytheon Co.
Chicago, Illinois

82415
Airpax Corp
Frederick Div.
Frederick, Maryland

82872
Roanwell Corp.
New York, New York

82877
Rotron Inc.
Custom Div.
Woodstock, New York

82879
ITT
Royal Electric Div.
Pawtucket, Rhode Island

83003
Varo Inc.
Garland, Texas

83014
Hartwell Corp.
Placentia, California

83055
Signalite Fuse Co.
(Now 71744)

83058
TRW Assemblies & Fasteners Group
Fasteners Div.
Cambridge, Massachusetts

83259
Parker-Hannifin Corp.
O-Seal Div.
Culver City, California

83298
Bendix Corp.
Electric & Fluid Power Div.
Eatonville, New Jersey

83315
Hubbell Corp.
Mundelein, Illinois

83330
Kulka Smith Inc.
A North American Philips Co.
Manasquan, New Jersey

83478
Rubbercraft Corp. of America
West Haven, Connecticut

83553
Associated Spring Barnes Group
Gardena, California

83740
Union Carbide Corp.
Battery Products Div.
Danbury, Connecticut

84171
Arco Electronics
Commack, New York

84411
American Shizuki
TRW Capacitors Div.
Ogallala, Nebraska

84613
FIC Corp.
Rockville, Maryland

84682
Essex Group Inc.
Peabody, Massachusetts

85367
Bearing Distributing Co.
San Fransisco, California

85372
Bearing Sales Co.
Los Angeles, California

85480
W. H. Brady Co.
Industrial Product
Milwaukee, Wisconsin

85932
Electro Film Inc.
Valencia, California

86577
Precision Metal Products Co.
Peabody, Massachusetts

86684
Radio Corp. of America
(Now 54590)

86928
Seastrom Mfg. Co. Inc.
Glendale, California

87034
Illuminated Products Inc.
(Now 76854)

88219
GNB Inc.
Industrial Battery Div.
Langhorne, Pennsylvania

88245
Winchester Electronics
Litton Systems-Useco Div.
Van Nuys, California

88486
Triangle PWC Inc.
Jewitt City, Connecticut

88690
Essex Group Inc.
Wire Assembly Div.
Dearborn, Michigan

89020
Amerace Corp.
Buchanan Crimptool Products Div.
Union, New Jersey

89265
Potter-Brumfield
(See 77342)

89536
John Fluke Mfg. Co., Inc.
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89597
Fredericks Co.
Huntingdon Valley, Penna.

89709
Bunker Ramo-Eltra Corp.
Amphenol Div.
Broadview, Illinois

89730
General Electric
Lamp Div.
Newark, New Jersey

90201
Mallory Capacitor Co.
Sub of Emhart Industries Inc.
Indianapolis, Indiana

90215
Best Stamp & Mfg. Co.
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90303
Duracell Inc.
Technical Sales & Marketing
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91094
Essex Group Inc.
Suflex/IWP Div.
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91247
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91293
Johanson Mfg. Co.
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91462
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91502
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91506
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91507
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91637
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Columbus, Nebraska

91662
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A Gulf Western Mfg. Co.
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91737
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(Now 08718)

91802
Industrial Devices Inc.
Edgewater, New Jersey

91833
Keystone Electronics Corp.
New York, New York

91836
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Tuckahoe, New York

91929
Honeywell Inc.
Micro Switch Div.
Freeport, Illinois

91934
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91984
Maida Development Co.
Hampton, Virginia

91985
Norwalk Valve Co.
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92914
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93332
Sylvania Electric Products
Semiconductor Products Div.
Woburn, Massachusetts

94144
Raytheon Co.
Microwave & Power Tube Div.
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94222
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94988
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95263
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95275
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95303
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95348
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95354
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96853
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99120
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99217
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99378
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99392
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Roxboro Div.
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99515
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99779
Bunker Ramo- Eltra Corp.
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Appendix 7A
Manual Change Information

INTRODUCTION

This appendix contains information necessary to backdate the manual to conform with earlier pcb configurations. To identify the configuration of the pcb's used in your instrument, refer to the revision letter (marked in ink) on the component side of each pcb assembly. Table 7A-1 defines the assembly revision levels documented in this manual.

NEWER INSTRUMENTS

As changes and improvements are made to the instrument, they are identified by incrementing the revision letter marked on the affected pcb assembly. These changes are documented on a supplemental change/errata sheet which, when applicable, is inserted at the front of the manual.

OLDER INSTRUMENTS

To backdate this manual to conform with earlier assembly revision levels, perform the changes indicated in Table 7A-1.

CHANGE #1

In Section 6, subsection 521, replace the parts list in Table 521-4 with the one shown in Figure 7A-1. Also replace the component location drawing in Figure 521-6 with the one shown in Figure 7A-2.

In Section 8, replace the -521 component location drawing in Figure 8-7 with the one shown in Figure 7A-1. Replace the -521 schematic diagram in Figure 8-7 with the one shown in Figure 7A-3.

Table 7A-1. Manual Status and Backdating Information

Ref Or Option No.	Assembly Name	Fluke Part No.	* To adapt manual to earlier rev configurations perform changes in desending order (by no.), ending with change under desired rev letter																						
			—	A	B	C	D	E	F	G	H	J	K	L	M	N	P								
A1	Main PCB		●	●	●	●	X																		
A2	Front Panel PCB	476028	●	●	X																				
A5	Time Base PCB	406926	●	●	X																				
-010	Battery PCB	475962	●	●	X																				
-310	520 MHz Direct PCB	476051	●	●	●	X																			
-331	1300 MHz Prescaler PCB	475913	●	●	●	●	X																		
-331	DC to DC Converter PCB	475889	●	●	●	X																			
-521	Digital Interface PCB	487454	●	●	●	1	X																		

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	⊗ DATA INPUT/OUTPUT PCB ASSEMBLY FIGURE 521-5 OPTION -521 (7220A-4007T)	487454	89536	487454	1		
CR1	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	1	1	
J4	CONNECTOR, 36-PIN	484733	00779	87406-1	1		
P5	CONNECTOR, 36-PIN	479493	00779	552817-1	1		
R1	RES, DEP. CAR, 100K +/-5%, 1/4W	348920	80031	CR251-4-5P100K	1		
RN1	RES, NETWORK, 33K	484741	89536	484741	1	1	
U1	⊗ IC, C-MOS, HEX NON INVERT BUFFERS	407759	04713	MC14503CP	1	1	
U2	⊗ IC, C-MOS, DUAL TYPE "D" FLIP-FLOP	340117	04713	MC14013CP	1	1	
U3	⊗ IC, C-MOS, QUAD, 2-INPUT NAND GATES	355198	04713	MC14011CP	1	1	
U4	IC, TRI-STATE HEX BUFFER	483800	89536	483800	1	1	
U5	⊗ IC, C-MOS, BCD TO DECIMAL DECODER	380741	01295	TP4028AN	1	1	
U6	IC, LO-PWR, SCHOTTKY TRI-ST OCTAL, BFR.	429902	12040	DM81LS95N	1	1	
W1	PLUG, JUMPER	416895	91506	8136-650P2	1		
	SOCKETS	376418	89536	376418	15		

Figure 7A-1. Option -521 Parts List

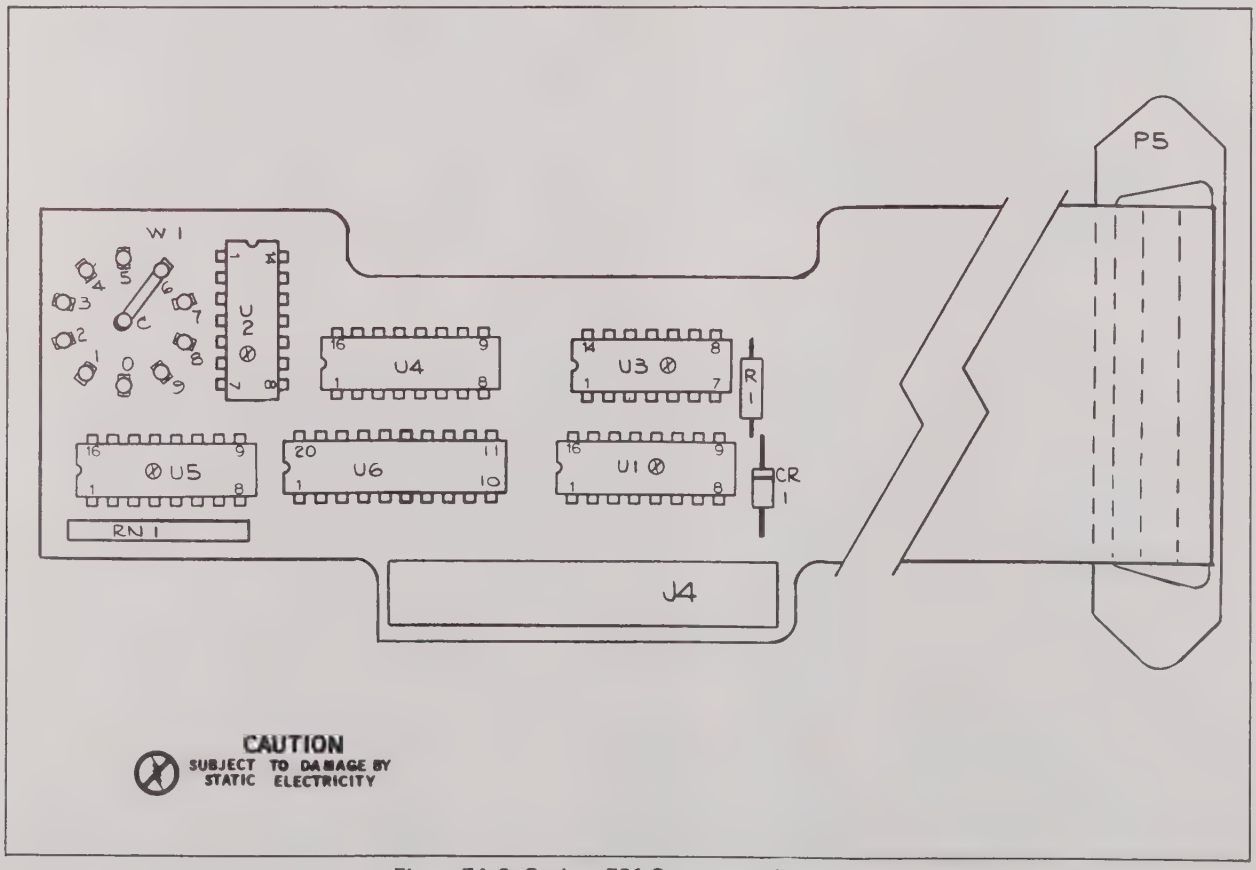

Figure 7A-2. Option -521 Component Locations

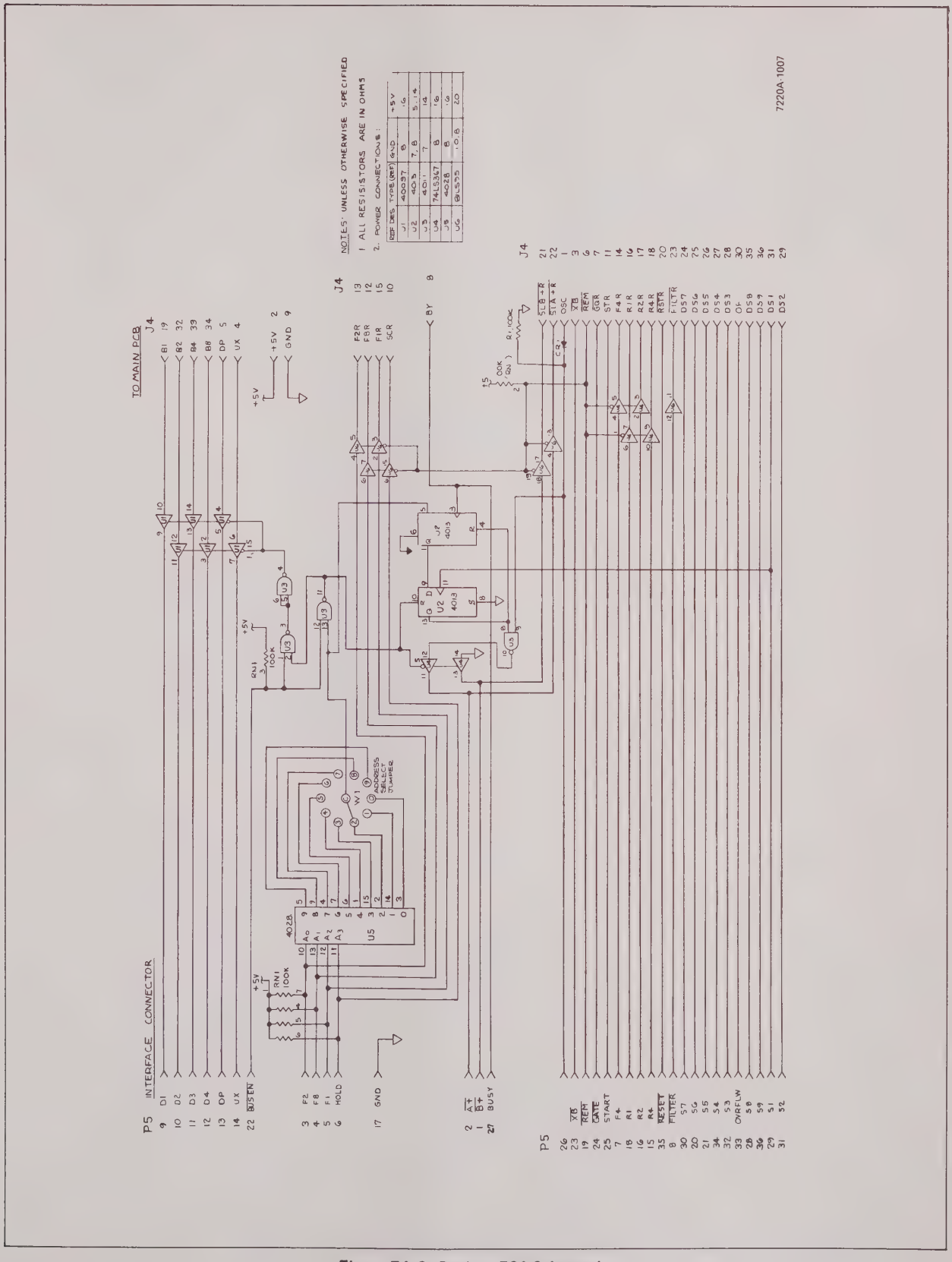

Figure 7A-3. Option -521 Schematic

Section 8
Schematic Diagrams

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AECL	Channel A Emitter Coupled Logic.
AO, AR	Autoranging Feedback Lines
A TTL	Channel A Transistor-Transistor Logic
B1, B2, B4, B8	Binary Coded decimal bits for each counter stage.
BECL	Channel B Emitter Coupled Logic.
B TTL	Channel B Transistor-Transistor Logic
BY (or B)	BUSY from Control Logic when measurement cycle is in progress.
$\overline{\text{C DIRECT}}$*	Channel C without presclaing.
C ECL	Channel C Emitter Coupled Logic
CI	Control Logic Clock Input – 1 MHz (1/6 MHz)
CO	TTL output from Control Logic. High in PER AVG A, CHK. 1 MHz to 10 Hz for TI A-B.
CPM	Counts Per Minute X100A function has been selected.
$\overline{\text{C SIG}}$*	Synchronized signal present on Channel C above threshold level - start measurement.
D1 through D6	Digit 1 through Digit 6.
D1 CARRY	Digit 1 carry.
DP	Decimal Point.
DS1 through DS8	Strobe 1 through Strobe 8.
EA	TTL Output from the Control Logic
EH	TTL ouptut from the Control Logic. Enables the 10 MHz.
F1, F2, F4, F8	Function Control Lines.
F1L, F2L, etc.	Function Control Lines from the Front Panel (Local).
F1R, F2R, etc.	Function Control Lines from the Remote Interface (Remote).
FC	FREQ C Function is selected.
$\overline{\text{FILT}}$*	100 kHz Low Pass Filter Control Line.
FILTL	Front Panel Enable of the Filter (Local).
FILTR	Remote Enable of the Filter (Remote).
$\overline{\text{G}}$*	Gate Annunciator Enable
GC	Main Gate Clock.
$\overline{\text{GR}}$*	Main Gate Reset.
$\overline{\text{GS}}$*	Main Gate Set.
GQ	Main Gate Enable
$\overline{\text{HE}}$*	Time Interval Holdoff Enable.
HLDAN	Time Interval Holdoff Analog.
M1, M2, M3	Control Logic Mode Inputs.
$\overline{\text{M}}$*	Update Memory.
OVEN	Oven energized.
$\overline{\text{OF}}$*	Overflow Annunciator Enable.
P1, P2	Control Logic Prescale Inputs.
PA	Period A Function.
PAV	Period Average A Function.
R	General Reset.
$\overline{\text{R}}$*	Reset Display and Decade Counters.
RØ	Resolution Range Zero - 10^0 /10 ns/10 kHz.
R1, R2, R3	Control Logic Resolution Range Inputs.
RI	Reset Input to the Control Logic.
$\overline{\text{REM}}$*	Remote Enable Line.
RRL	Range Reset Line.
$\overline{\text{RSTR}}$*	Remote Reset.
SCR	Remote Control Line for Single/Continuous selection.
SC	Single/Continuous Selection Line.
$\overline{\text{SLA}+}$*	Channel A Positive Slope Selection
$\overline{\text{SLA}-}$*	Channel A Negative Slope Selection
$\overline{\text{SLB}+}$*	Channel B Positive Slope Selection
$\overline{\text{SLB}-}$*	Channel B Negative Slope Selection
ST	Start Command
STR	Start Command from the Remote Interface
TI	Time Interval Function
TIA	Time Interval Average Function
TL	Trigger Light
TE	TTL Output from the Control Logic, high in TI
TQ	TTL Output from the Time Interval F/F. High at the end of measurements.
UX	Units Annunciation Control Line
XA	ECL Output of the Channel A Signal Conditioner
XB	ECL Output of the Channel B Signal Conditioner
X1, X2, X4, X8	First Decade Counter Output to 520 MHz Direct PCB.
X10	Times 10 attenuation of the input signal
X100	Times 100 attneuation of the input signal
Y1, Y2, Y4, Y8	D1/B1, B2, B4, B8 } inputs from the 520 MHz Direct PCB
Z1, Z2, Z4, Z8	D2/B1, B2, B4, B8 } inputs from the 520 MHz Direct PCB

* Negative True Logic

Figure 8-1. Mnemonics

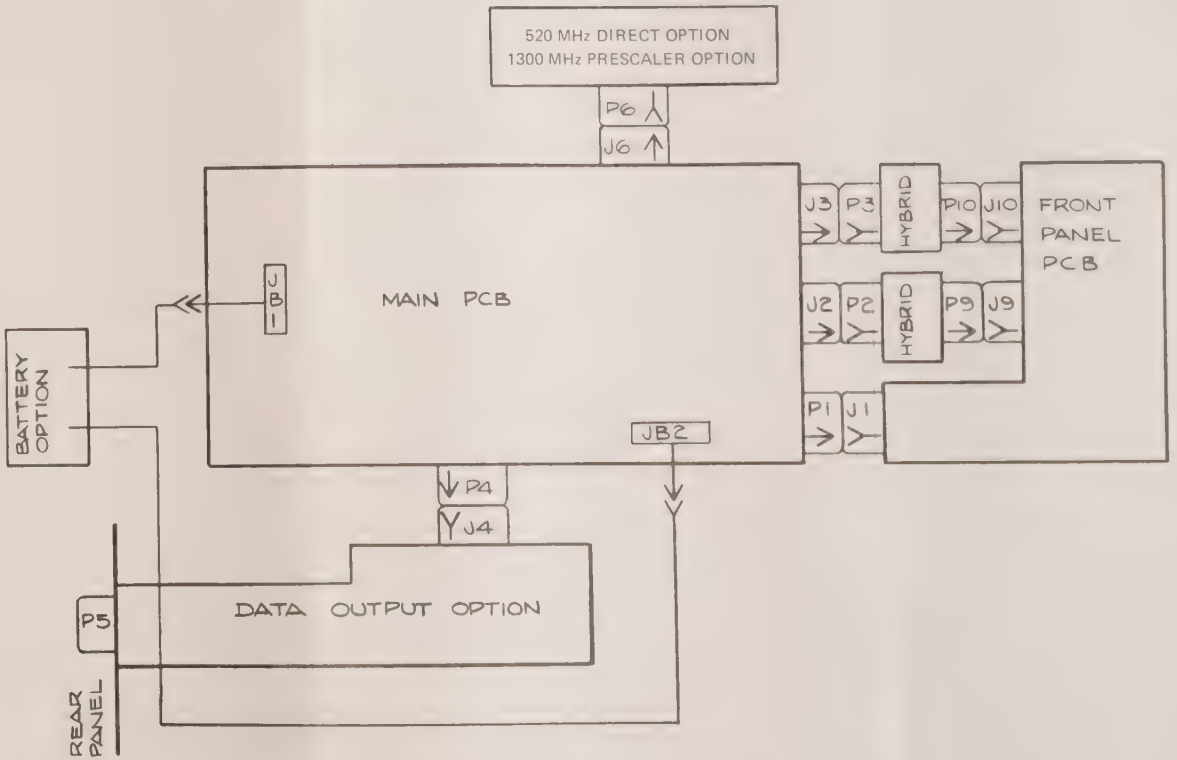


Figure 8-2. 7260A Interconnect Diagram

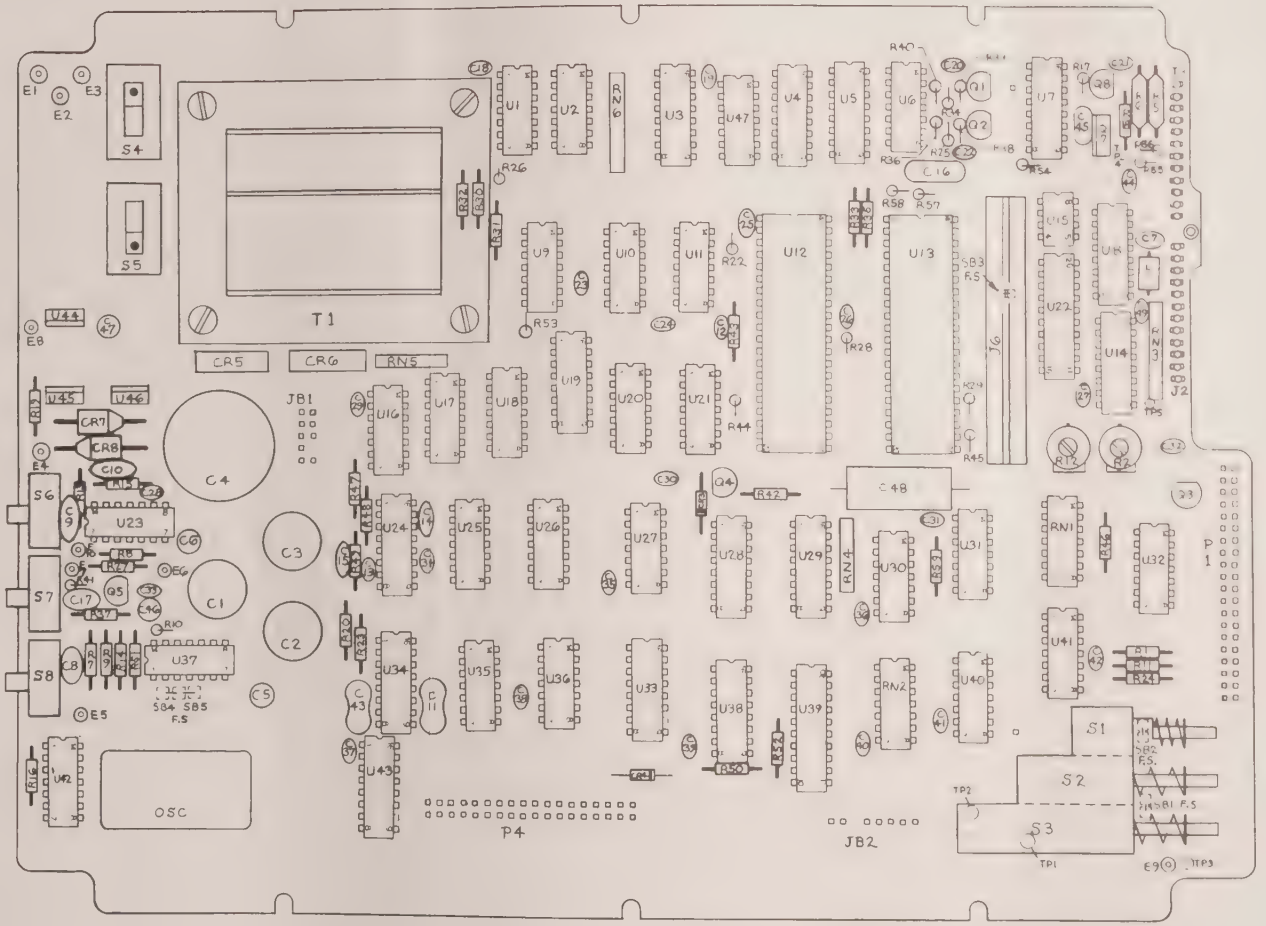
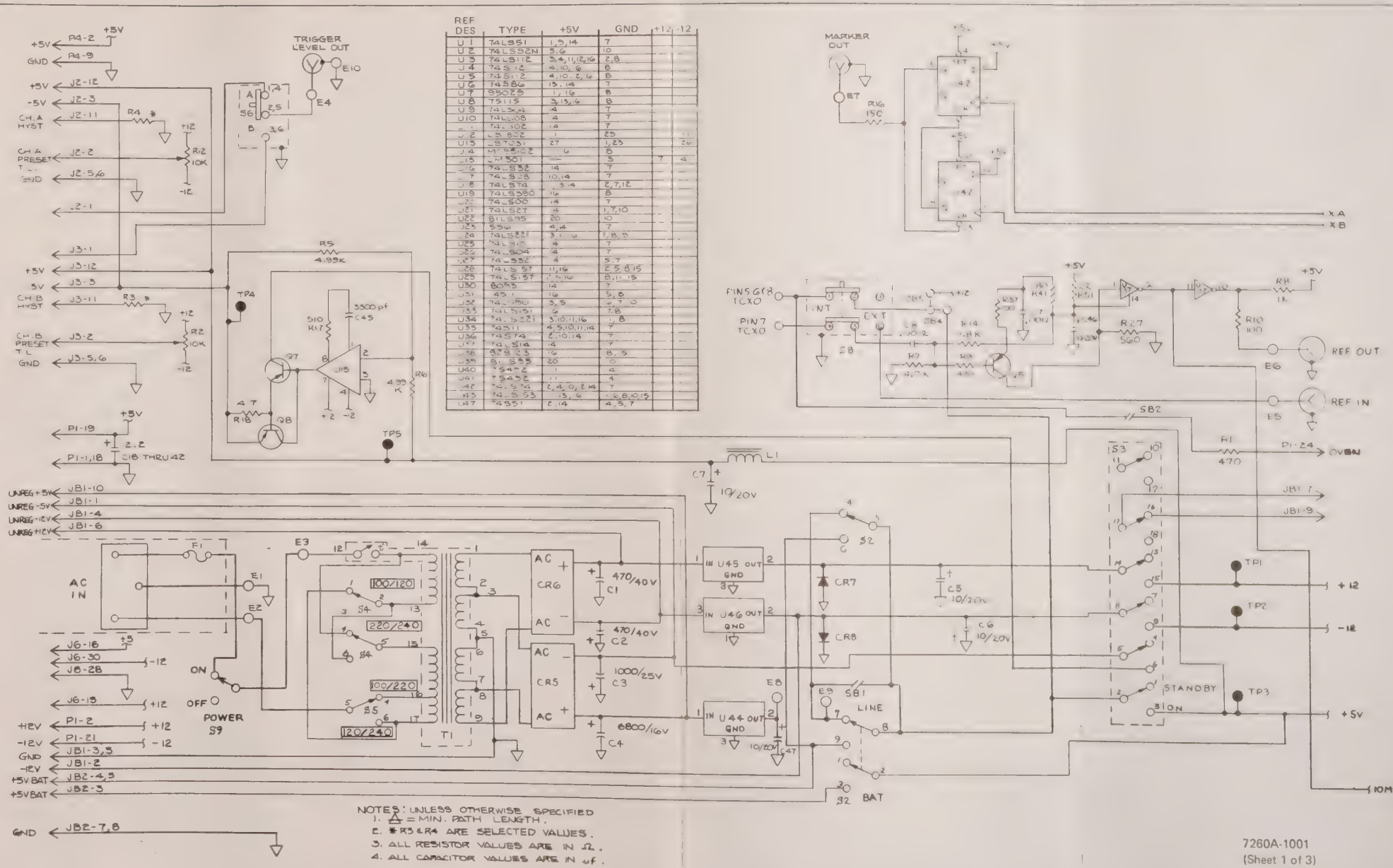


Figure 8-3. A1 Main PCB Assembly



REF DES	TYPE	+5V	GND	+12	-12
U1	74LS51	1,5,14	7		
U2	74LS32N	5,6	10		
U3	74LS112	5,4,11,12,16	2,8		
U4	74S112	4,10,6	8		
U5	74S112	4,10,2,6	8		
U6	74S86	13,14	7		
U7	95025	1,16	8		
U8	75115	3,13,6	8		
U9	74LS04	4	7		
U10	74LS08	4	7		
U11	74LS02	14	7		
U12	LS 802	1	25		
U13	LS7031	27	1,23		24
U14	MC6812	6	8		
U15	74S01	—	3	7	4
U16	74LS32	14	7		
U17	74LS08	10,14	7		
U18	74LS74	13,14	2,7,12		
U19	74LS3280	16	8		
U20	74LS00	14	7		
U21	74LS27	4	1,7,10		
U22	81LS95	20	10		
U23	5516	24	12		
U24	74LS221	3,16	1,8,9		
U25	74LS10	4	7		
U26	74LS04	4	7		
U27	74LS32	4	5,7		
U28	74LS157	11,16	1,5,8,15		
U29	74LS157	11,16	8,11,15		
U30	8095	12	7		
U31	451	16	5,8		
U32	74LS00	3,5	6,7,10		
U33	74LS151	6	7,8		
U34	74LS221	3,10,11,16	1,8		
U35	74S11	4,5,10,11,14	7		
U36	74S74	2,10,14	7		
U37	74LS14	14	7		
U38	8223	16	8,5		
U39	81LS95	20	10		
U40	7442	1	8		
U41	7445	11	4		
U42	74S74	2,4,10,12,14	7		
U43	74LS53	13,6	4,8,10,12		
U47	74S51	2,14	4,5,7		

NOTES: UNLESS OTHERWISE SPECIFIED
1. △ = MIN. PATH LENGTH.
2. *R3 & R4 ARE SELECTED VALUES.
3. ALL RESISTOR VALUES ARE IN Ω.
4. ALL CAPACITOR VALUES ARE IN uf.

7260A-1001
(Sheet 1 of 3)

Figure 8-3. A1 Main PCB Assembly (cont)

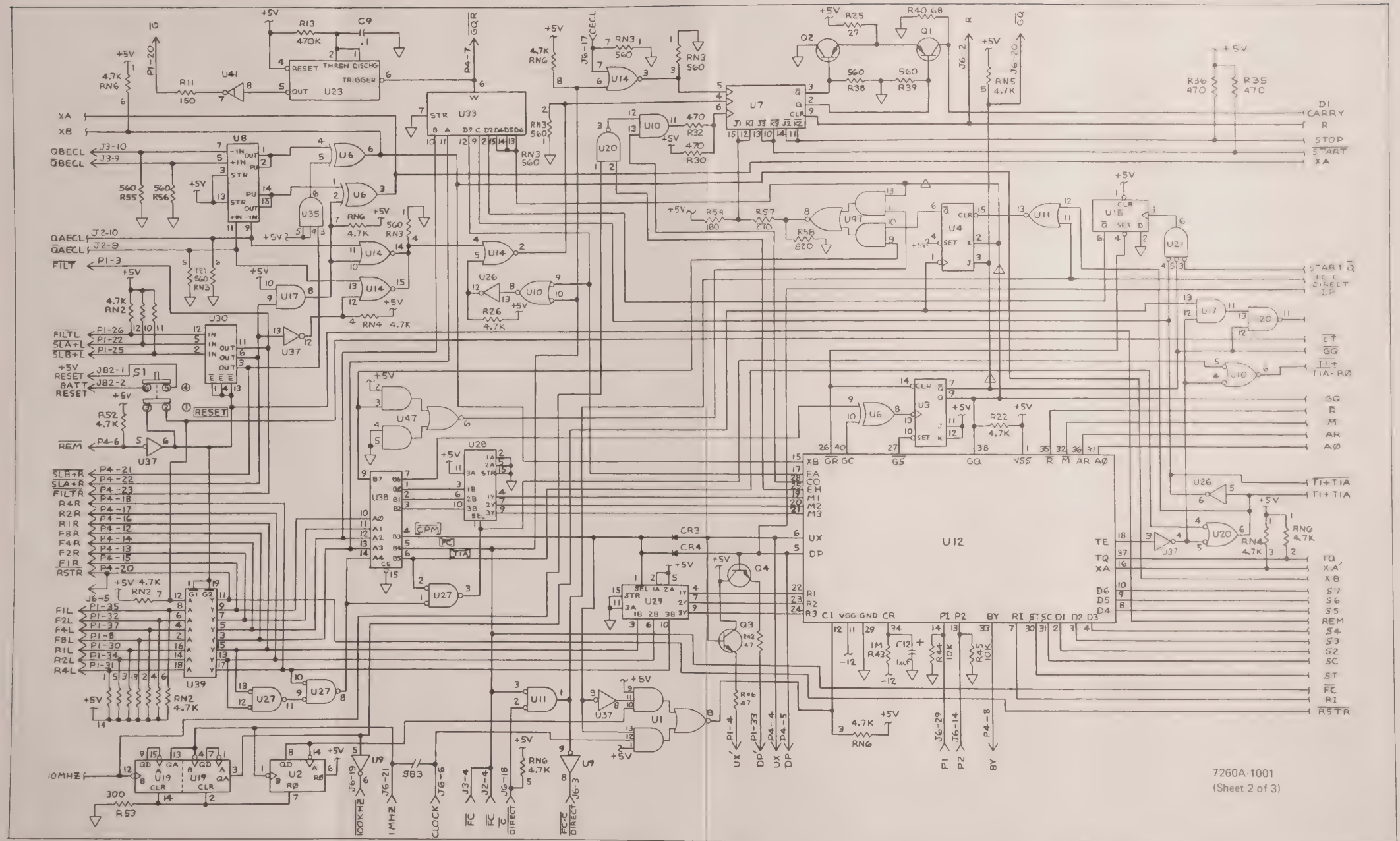


Figure 8-3. A1 Main PCB Assembly (cont)

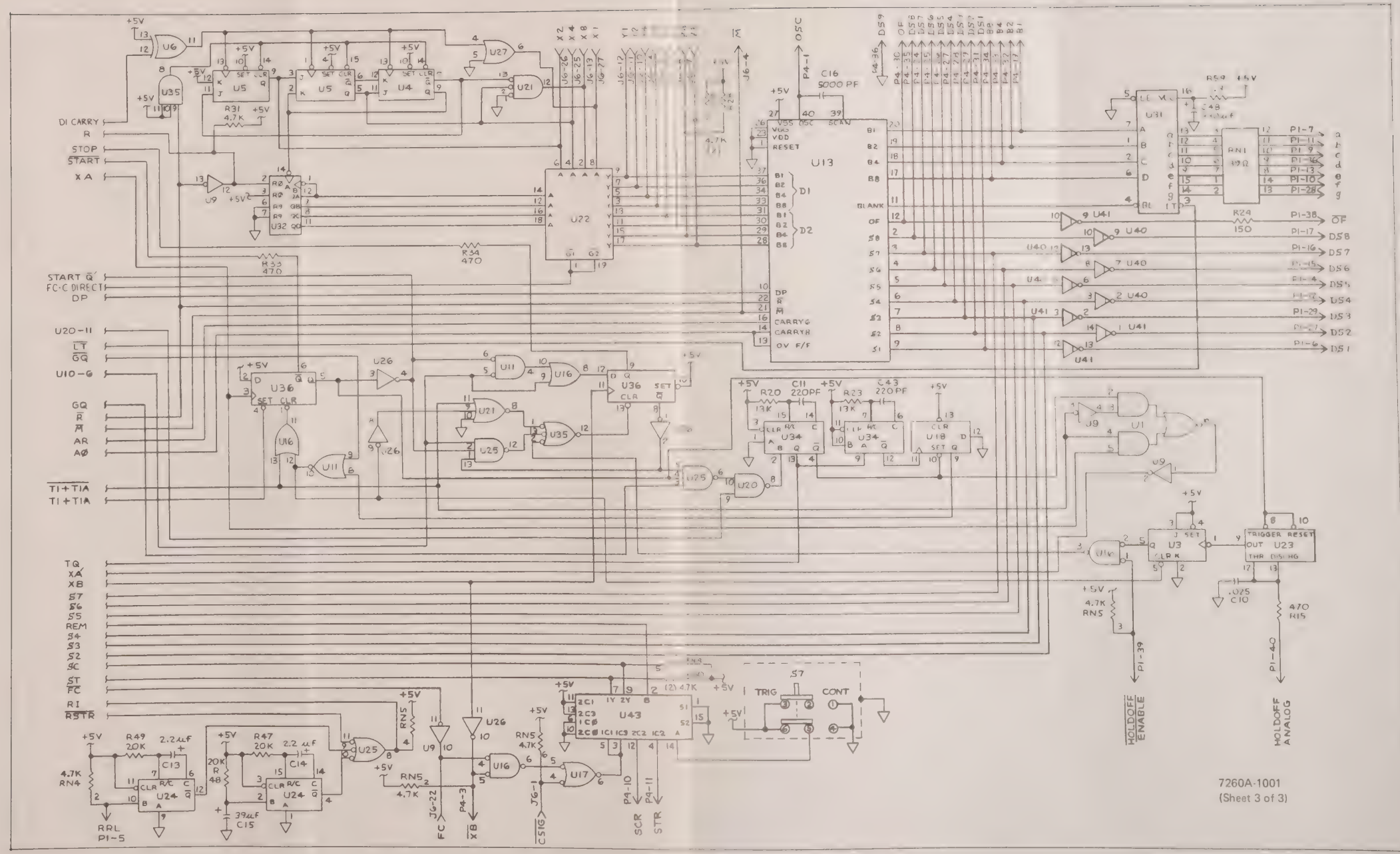


Figure 8-3. A1 Main PCB Assembly (cont)

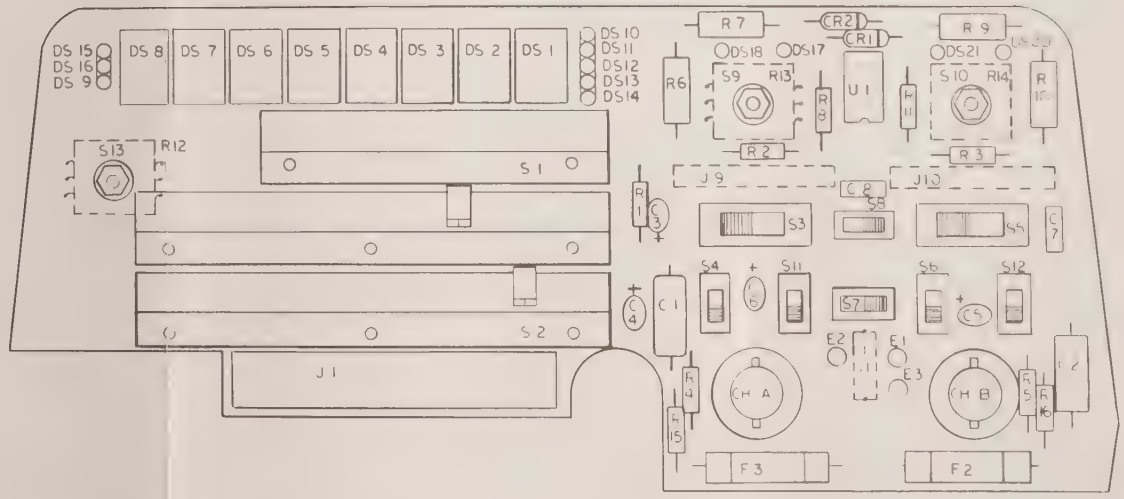


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Figure 8-4. A2 Front Panel PCB Assembly

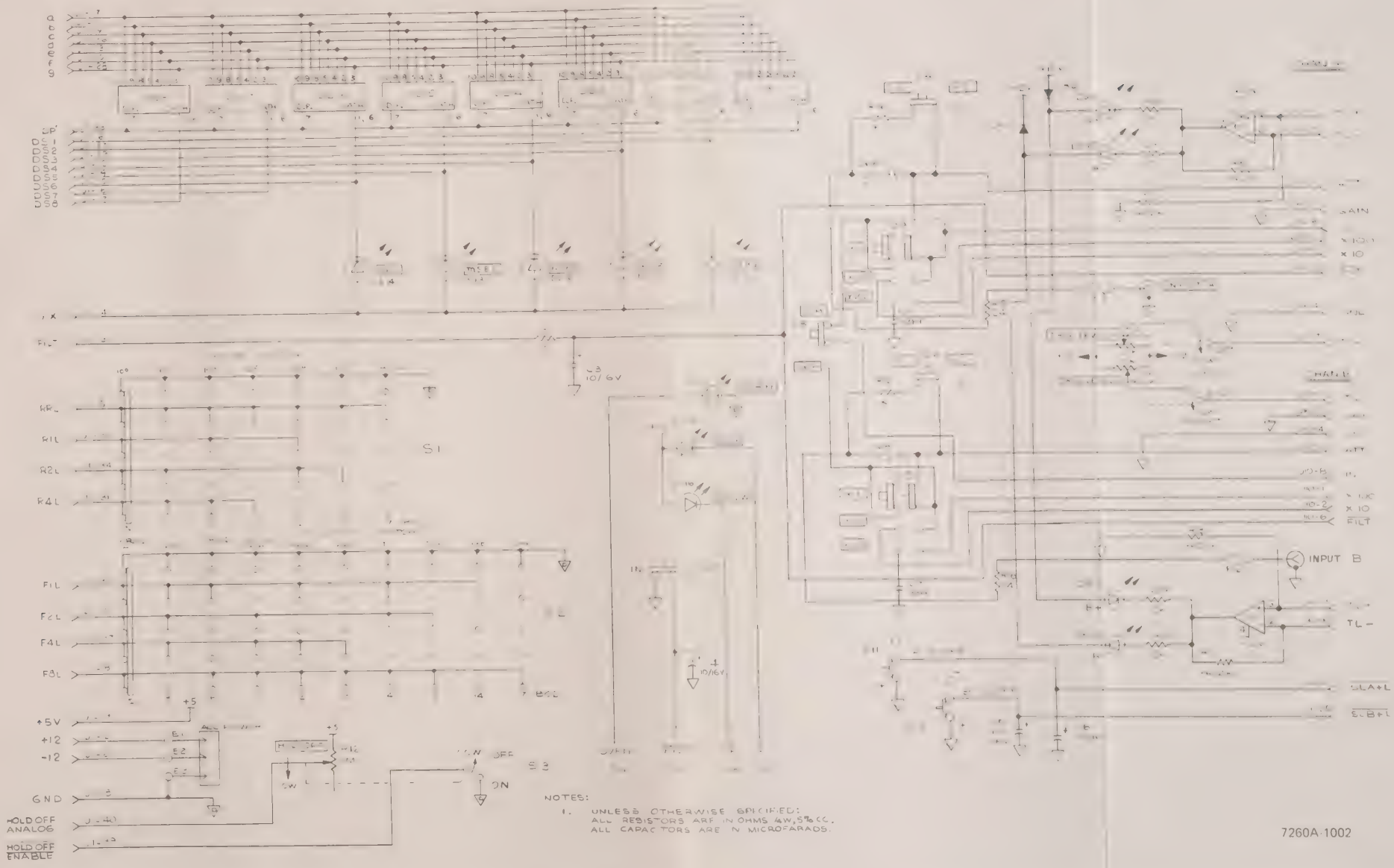

Figure 8-2. A2 Front Panel PCB Assembly (cont)

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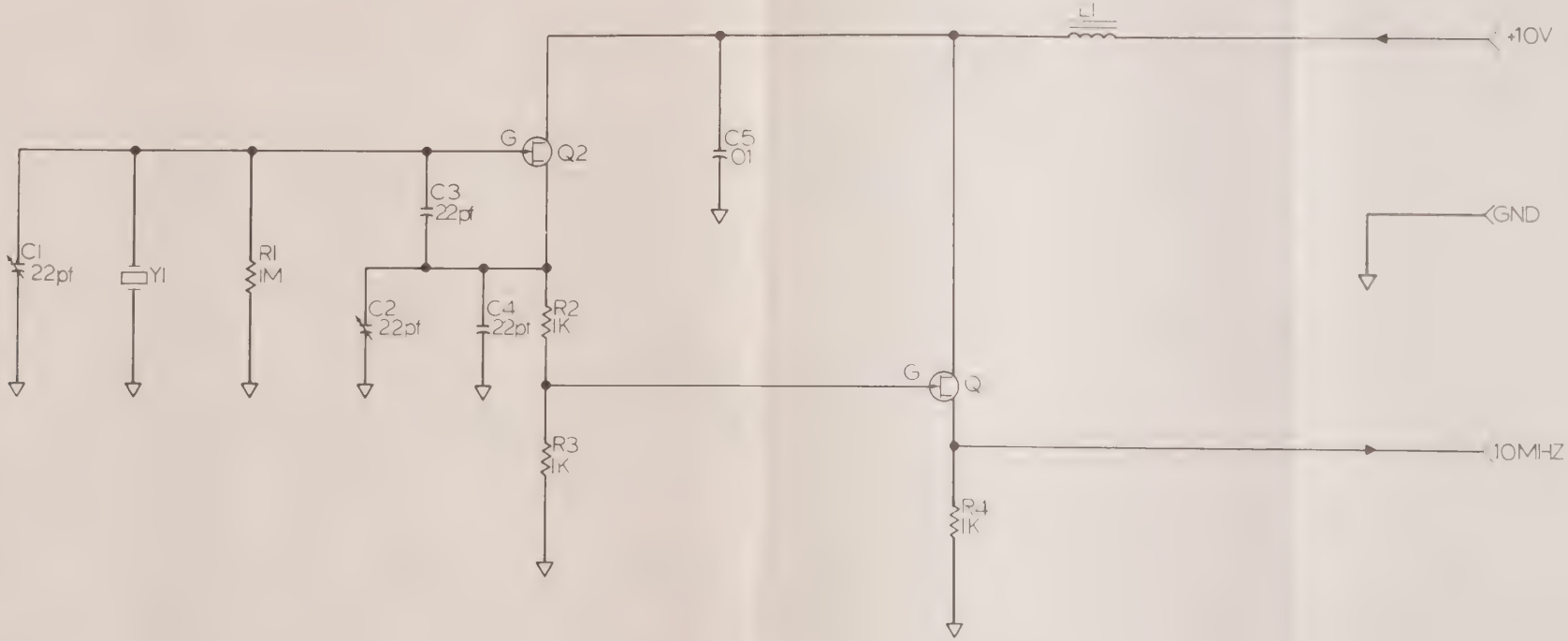

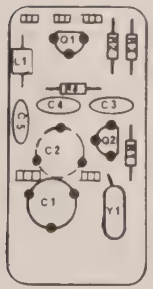

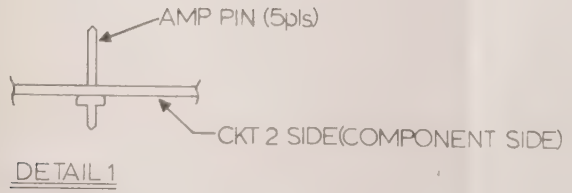

DETAIL 1

1952B-1010

Figure 8-5. A5 Time Base PCB Assembly

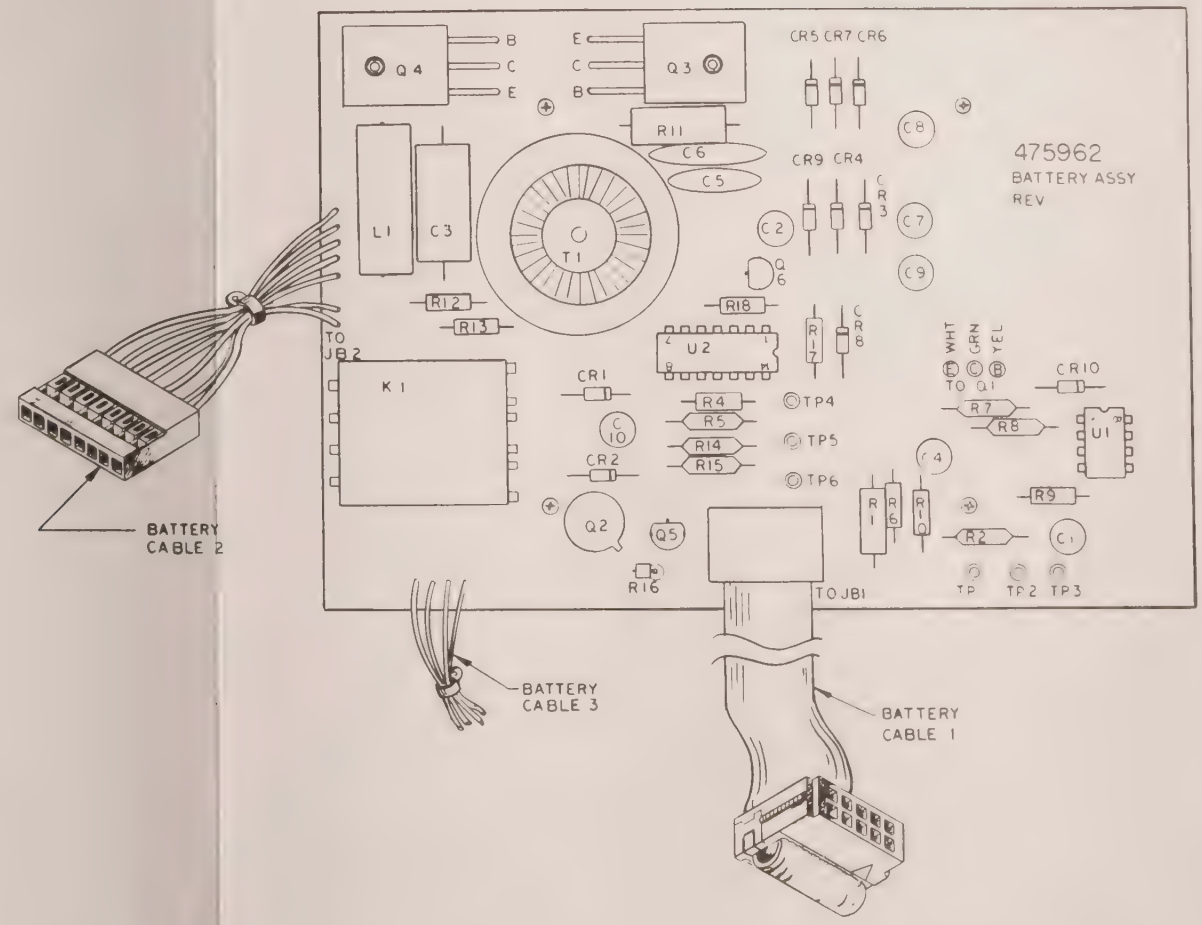

Figure 8-6. Battery PCB Assembly, Option -010

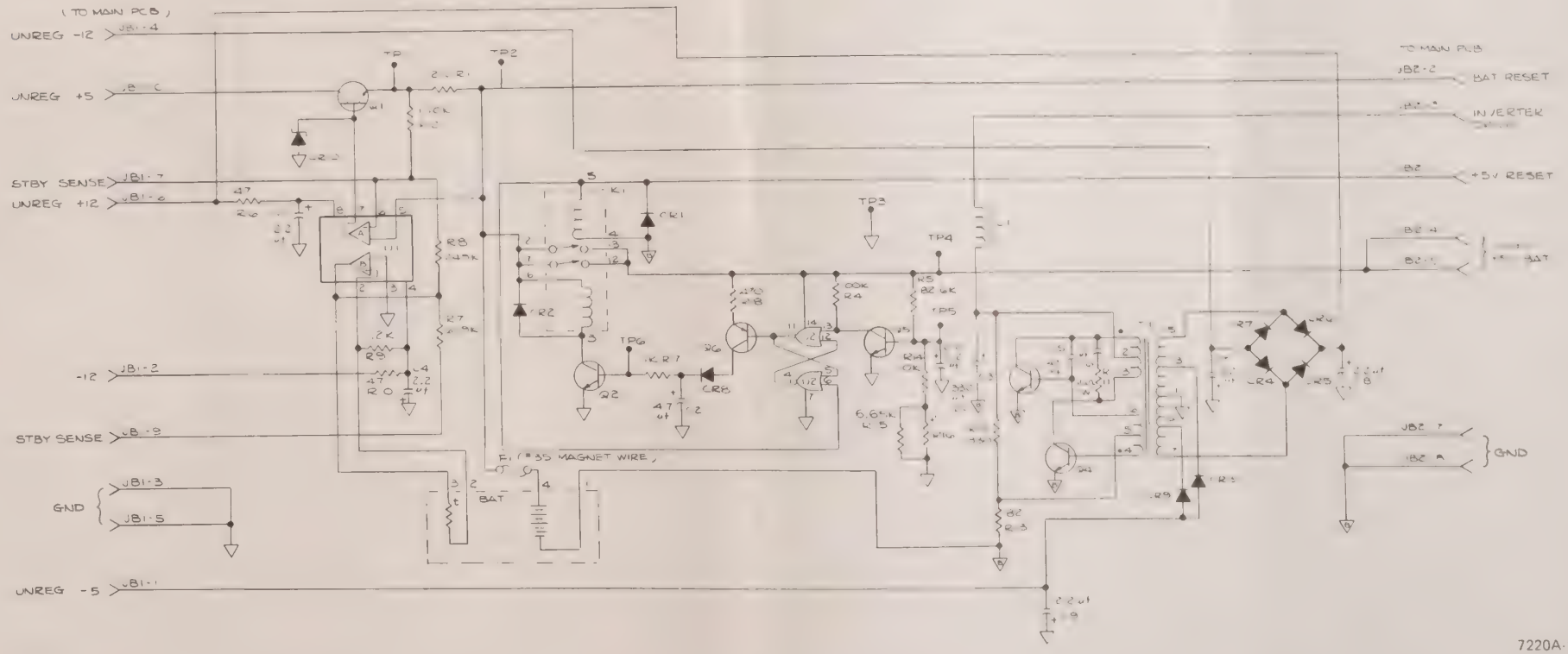

Figure 8-6. Battery PCB Assembly, Option -010 (cont)

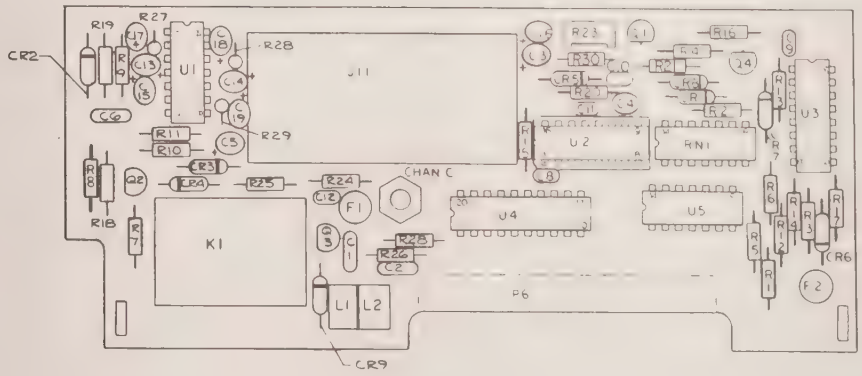

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Figure 8-7. Channel C Direct PCB Assembly, Option -310

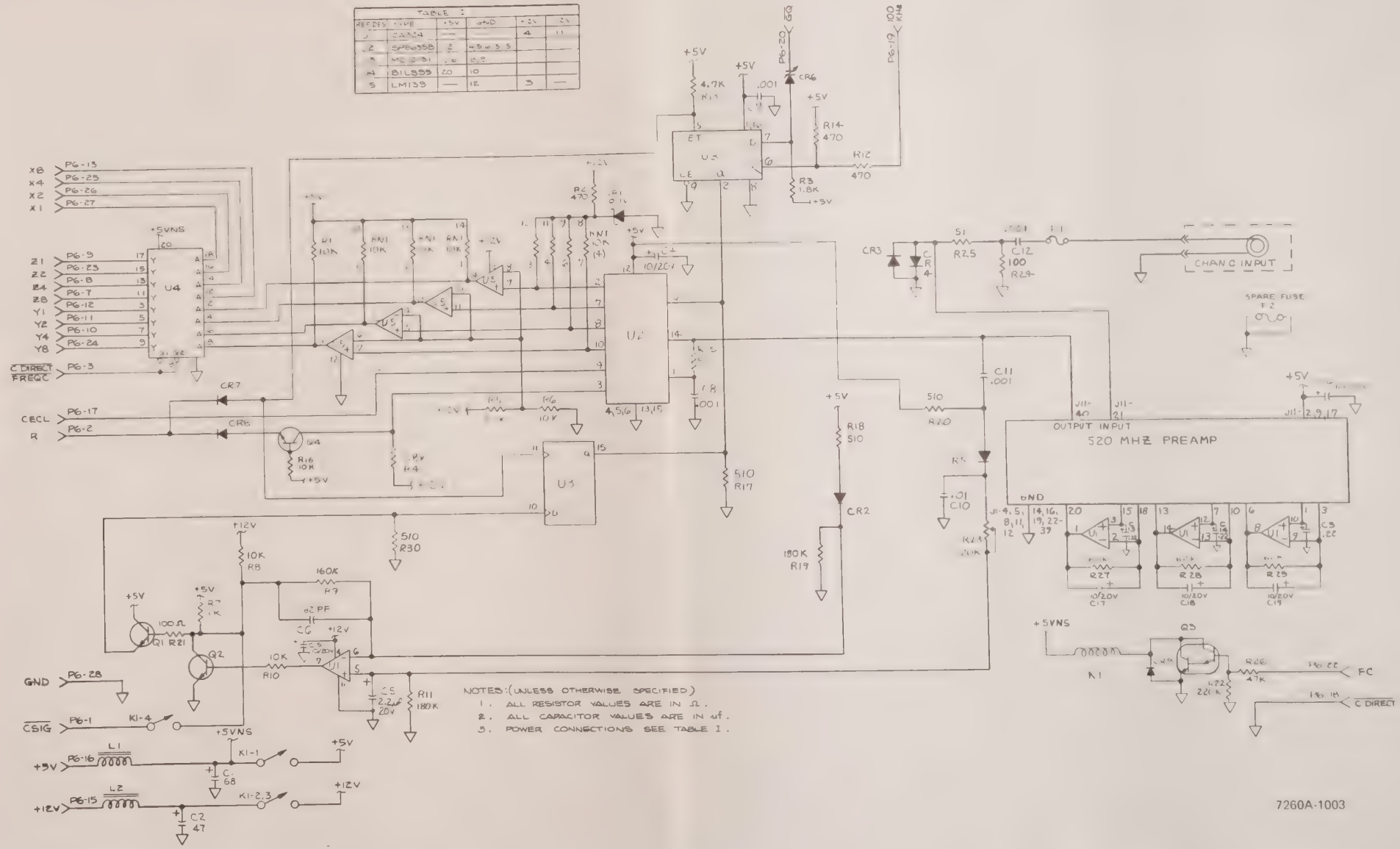
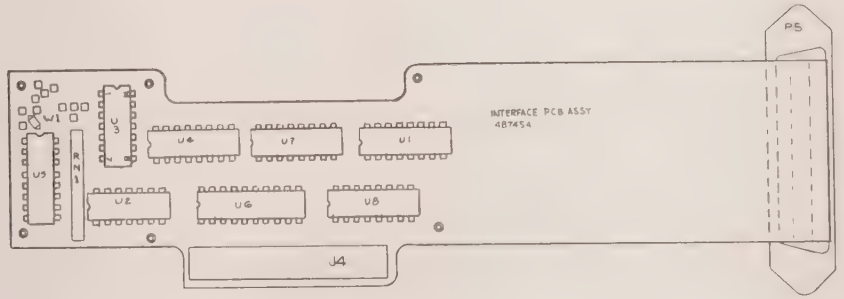


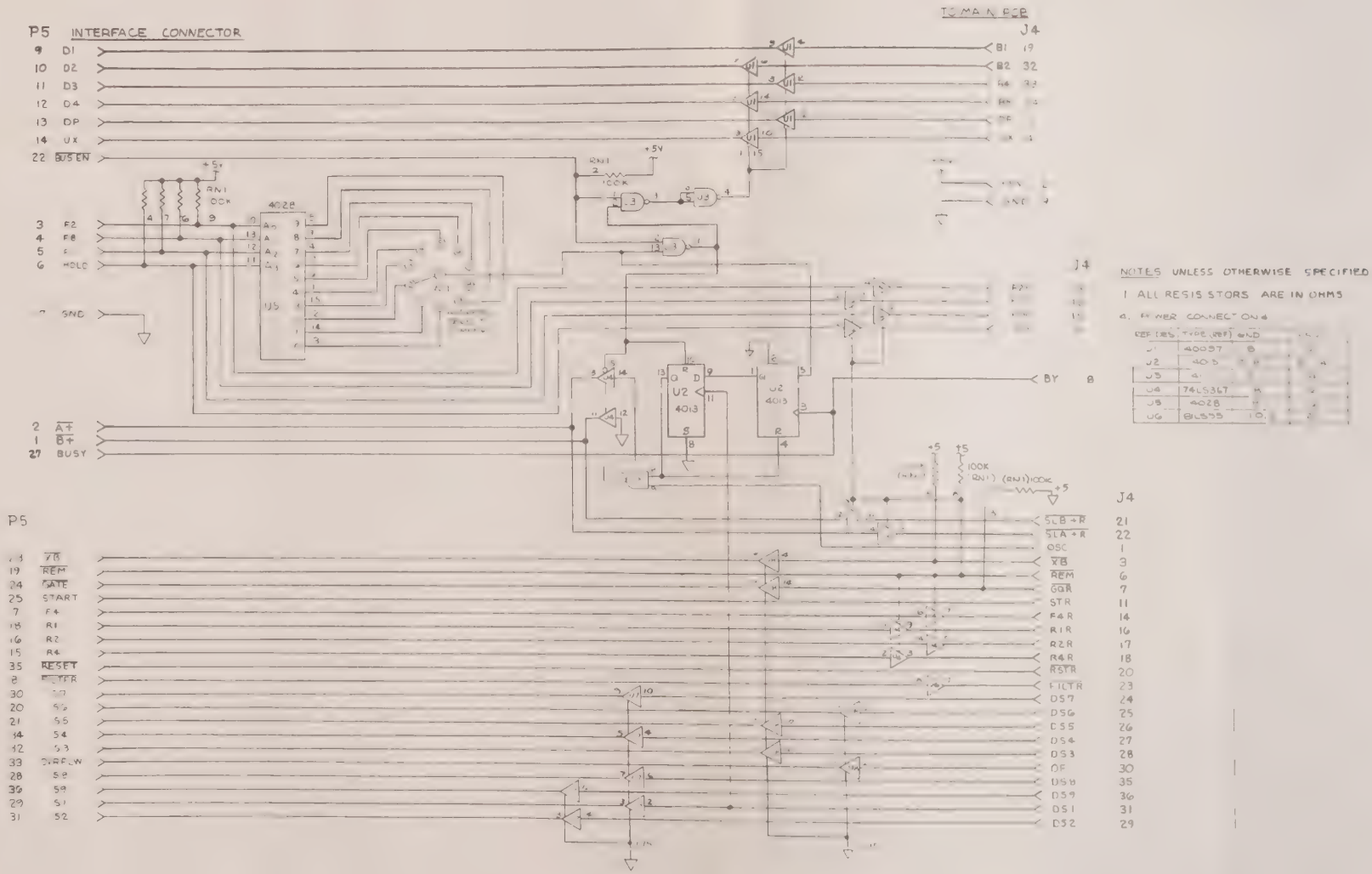
TABLE I
REFDES | TYPE | +5V | GND | +12V | -12V
U1 | 2N2484 | — | — | 4 | 11
U2 | SP8635B | 2 | 4 5 6 8 | | |
U3 | MC1431 | 16 | 8 12 | | |
U4 | 8ILS93 | 20 | 10 | | |
U5 | LM139 | — | 12 | 3 | —
NOTES:(UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTOR VALUES ARE IN Ω.
2. ALL CAPACITOR VALUES ARE IN uf.
3. POWER CONNECTIONS SEE TABLE I.
520 MHZ PREAMP
OUTPUT INPUT
CHAN C INPUT
SPARE FUSE F2
C DIRECT FREQC
CECL R
CSIG
7260A-1003

Figure 8-7. Channel C Direct PCB Assembly, Option -310 (cont)



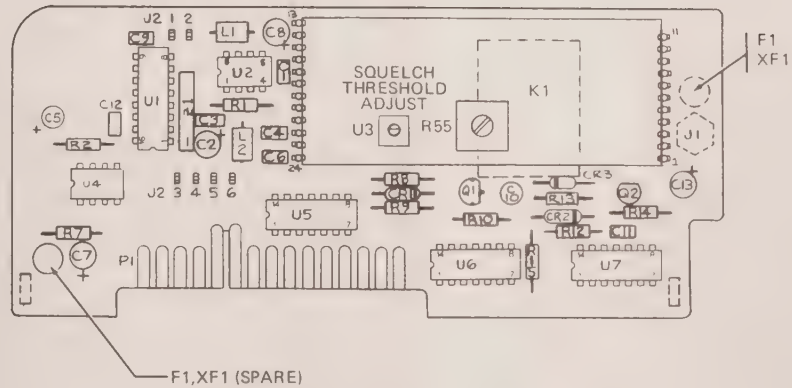
7220A-1607

Figure 8-8. Digital Interface PCB Assembly, Option -521



7220A-1007

Figure 8-8. Digital Interface PCB Assembly, Option -521 (cont)



7260A1604

Figure 8-9. 1300 MHz Prescaler PCB Assembly, Option -331

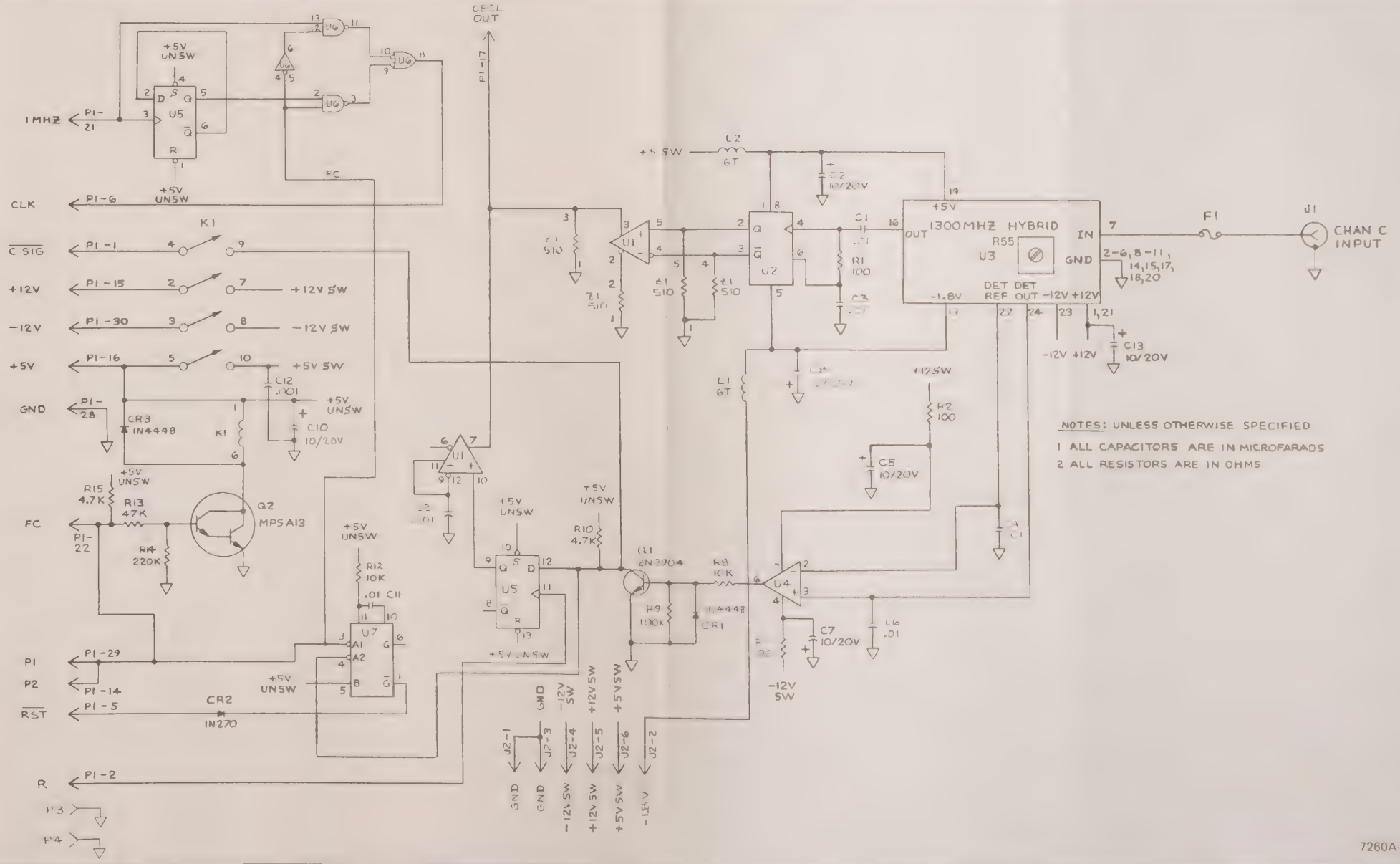
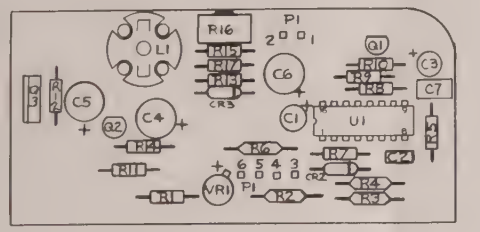


Figure 8-9. 1300 MHz Prescaler PCB Assembly, Option -331 (cont)



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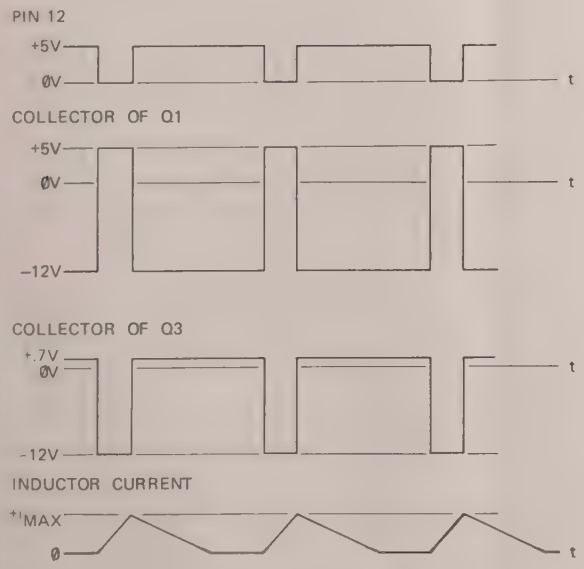
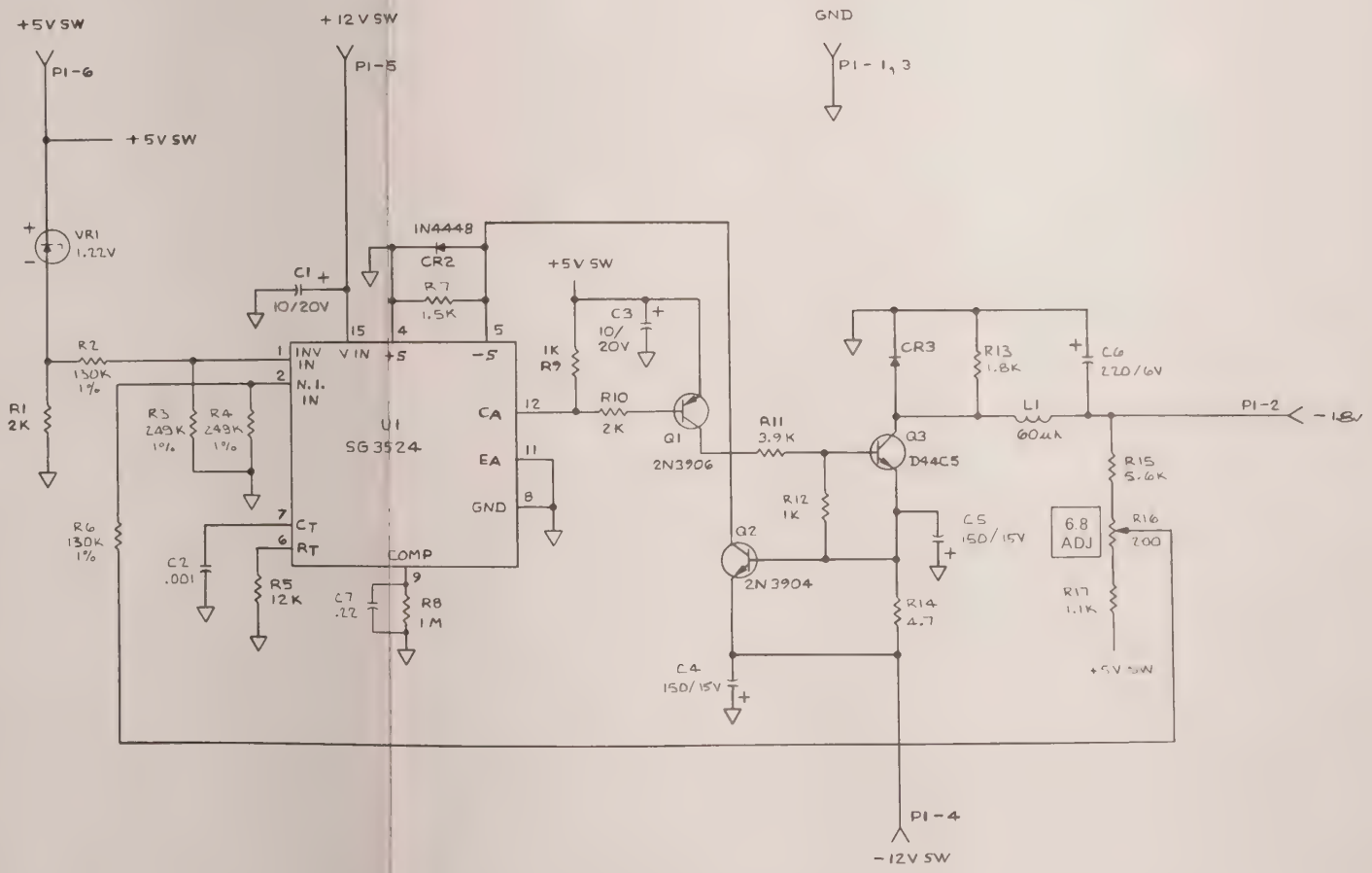


VOLTAGE WAVEFORMS



NOTES: UNLESS OTHERWISE SPECIFIED

1 ALL CAPACITANCE IN MICROFARADS.
2 ALL RESISTANCE IN OHMS.

7260A-1005

Figure 8-10. DC to DC Converter PCB Assembly, Option -331

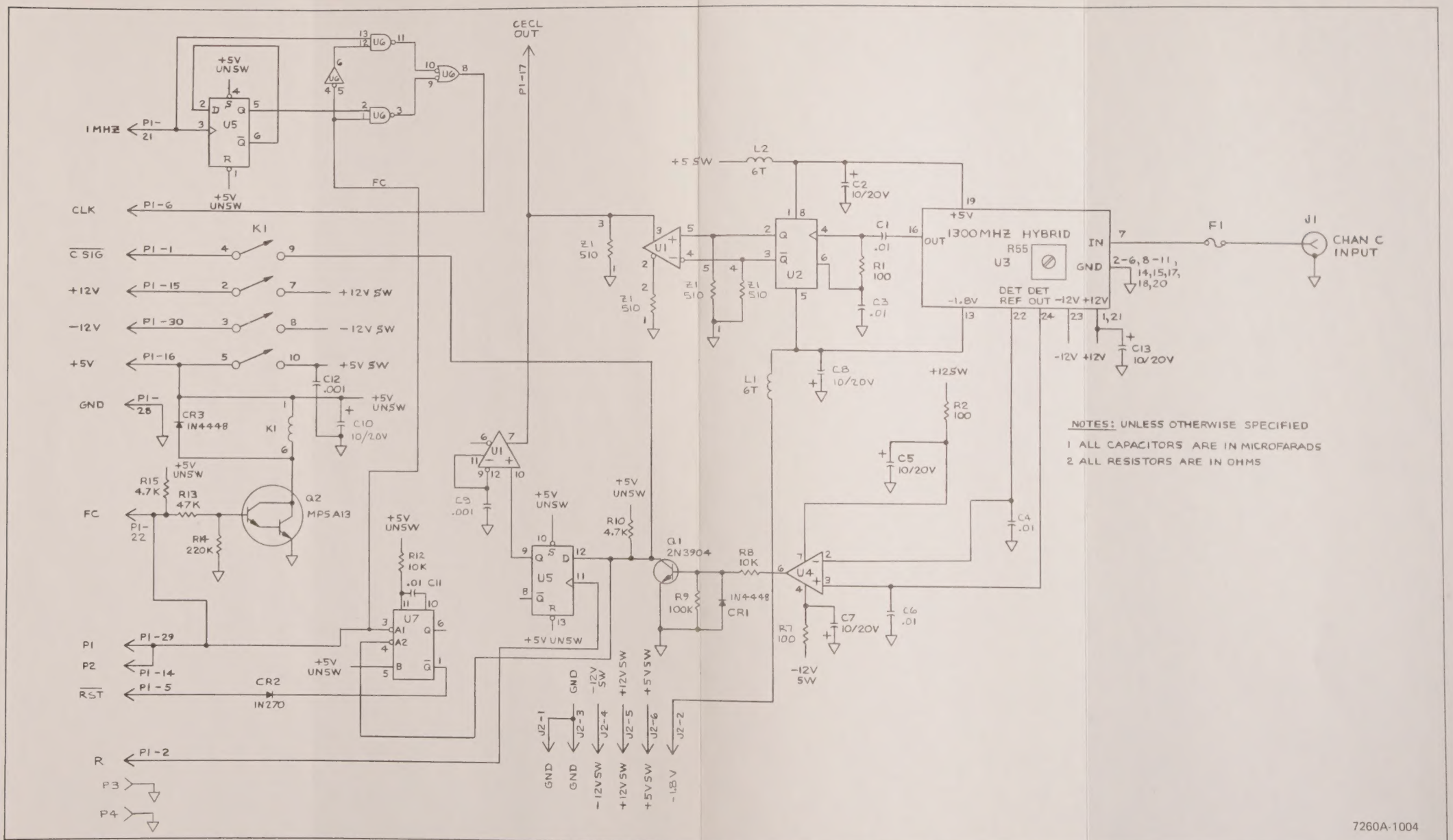
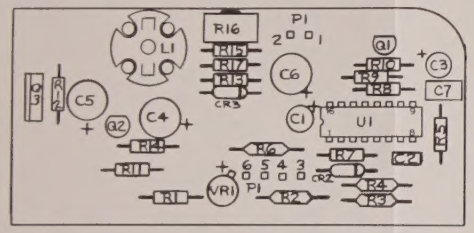
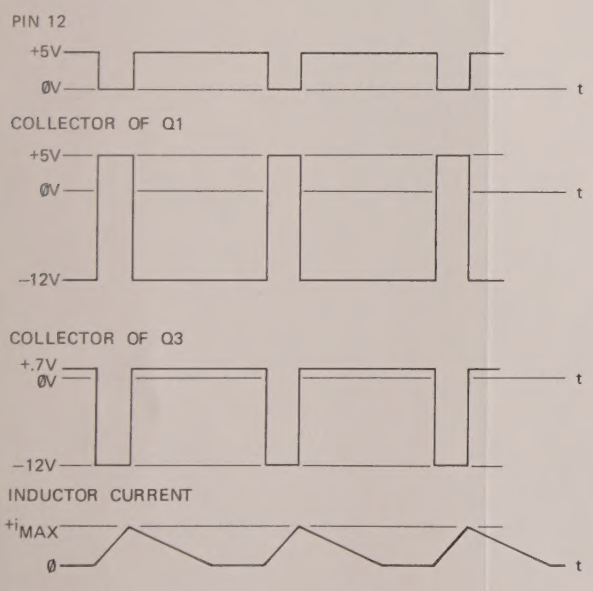


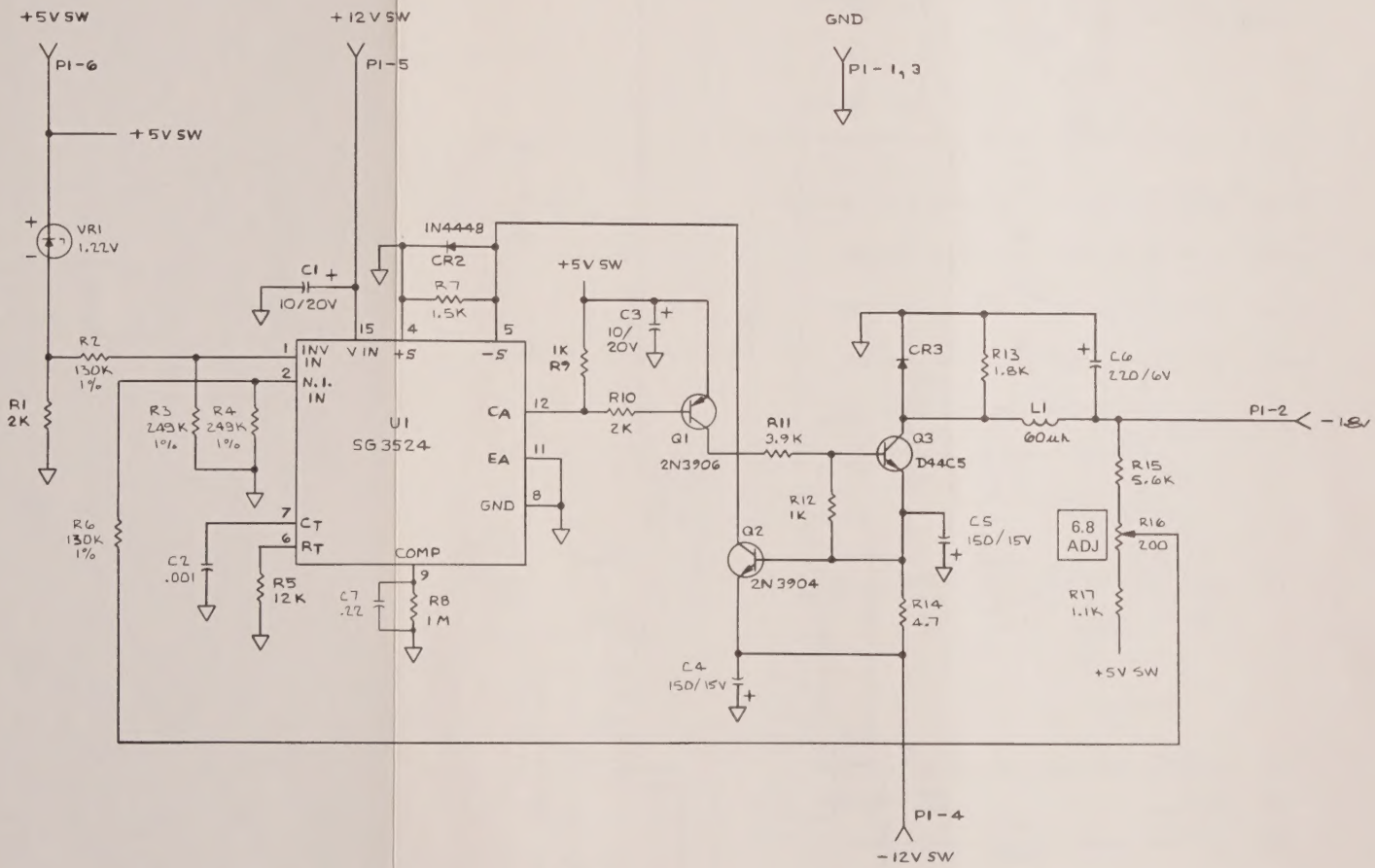
Figure 8-10. 1300 MHz Prescaler PCB Assembly (cont)



7260A-1605



VOLTAGE WAVEFORMS



NOTES: UNLESS OTHERWISE SPECIFIED

1 ALL CAPACITANCE IN MICROFARADS.
2 ALL RESISTANCE IN OHMS.

7260A-1005

Figure 8-11. DC to DC Converter PCB Assembly

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